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Research Article

A Research Study for the Design of a Portable and Configurable Ground Test System for the A400M Aircraft

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This paper presents a study of the most suitable ground test equipment for the Airbus A400M aircraft aimed at optimizing a design that combines portability, flexibility, and configurability. The study is based on current trends in the configuration of the different parts that are involved in the process of designing Aircraft Interface Modules (AIMs). Researches have been conducted facing the real problems of data acquisition and control in the assembly, maintenance, and repair processes of aircraft. In this sense, the number of signals used simultaneously in historical tests has been determined to be a parameter that plays an important role in the analysis. This work is within the framework of a project that our working group of the Department of Electronic Technology has carried out together with the company Airbus Defense and Space (Airbus DS). Thus, all the analyses and researches for the different configurations of the test equipment have been validated for the company. Some state-of-the-art systems have been considered in the process of designing the structure of the test system while analyzing the main advantages and drawbacks. Every hardware or software component was identified and justified according to its importance with respect to the use case. A comparison of how every approach meets the requirements was taken into account to define a methodology for designing a portable and configurable ground testing system. Thus, the conclusions of our study are being used by Airbus DS for the design of a prototype for the next generation of AIMs in A400M.

1. Introduction

Airbus Defense and Space (Airbus DS) is a company belonging to the Airbus Group that is dedicated to four main lines of business: military aerial systems, space systems, electronics and communications, and intelligence and security.

Currently, Airbus DS has several centers in Spain; specifically, there are three plants in Seville: Tablada, San Pablo Norte, and San Pablo Sur. The last is known as the FAL (Final Assembly Line—final assembly plant) and is where several models of aircraft are assembled, such as the A400M, C-295, CN-235, and C-212.

In the case of the A400M, a military transport aircraft, the assembly procedure at the FAL is based on a structure of different stations. Each station is dedicated to a specific purpose. For example, there is a station dedicated to the assembly of the wings, another one dedicated to motors, etc. There is a specific station that is the main plant dedicated for ground tests and is where all the equipment, systems, wires, etc. are tested. In this station, the aircraft must undergo a series of verification tests of its assembly before commissioning [1]. In addition, once the aircraft is in production, it is also necessary to check routinely for faults and to perform various tests to verify its correct operating status [2–6].

These tests must be carried out in accordance with a set of established procedures, either by the specific regulations of each country, the scope of application, or the client's requirements. The tests depend both on the application to which the aircraft is dedicated to or on its characteristics. There are huge differences in the tests given to various types of aircraft, such as civil, military, light, and heavy.

In addition, the tests of each subsystem of a particular aircraft require the reading of various parameters, such as temperature, pressure, vibration, voltage, current, linear speed, and rotation speed. Therefore, contrary to tests in other areas of application, in many companies in the aeronautical sector,

the tests are mainly carried out manually [2], using several tools and without automated procedures. Consequently, important tasks such as traceability and analysis are difficult to perform.

In this sense, Airbus has recently partnered with the Department of Electronic Technology at the University of Seville to develop the project "AI2X: Sistema Integral Avanzado de Verificaciones Aeronáuticas." AI2X is a collaboration among Airbus DS, various companies, and our research organization. The objective of this paper is to research, compare, and study the most suitable ground test equipment according to certain design requirements. Specifically, the work studies the procedure of configuring a generic and portable ground testing system for the A400M aircraft. After all, this system constitutes a generic and flexible AIM (Aircraft Interface Module). This AIM must combine a series of features aimed at facilitating its use by maintenance technicians. These features are as follows:

(i) *Size and Portability*. An adequate ergonomics analysis is required. This equipment must be able to validate a multitude of tests of different technologies, and it must be portable. These tests are not carried out in a production plant, so not all means are available

(ii) *Robustness*. Data acquisition systems and signal analyses are available on the market; however, these are not indicated for an industrial environment. Therefore, restructuring of these solutions must be considered to make them robust

(iii) *Modularity*. The maintenance or update operations are programmed in time, and in each case, some can be performed and others cannot. Therefore, the system must be configurable in such a way that tests can be prepared easily so that it is possible, in a small space, to access the various interfaces that the plane handles

(iv) *Connectivity*. One of the fundamental aspects will be this condition. The system must allow the tests to be registered so that the maintenance information can be easily retrieved, even by the customer

(v) *Standardization*. The system will allow having equipment of generic spare parts, lowering costs, and simplifying the maintenance tasks

(vi) *Versatility*. Being able to use the same equipment to give different solutions is a necessary requirement to provide flexibility to the system

(vii) *Ease of Configuration*. This allows the system to easily adapt to different needs and tests

The paper is organized as follows. Section 2 introduces some state-of-the-art traditional test systems. Portable and configurable test systems for aviation are presented in Section 3. A discussion based on the Airbus A400M aircraft is presented in Section 4. Finally, Section 5 concludes with some reflections and final remarks.

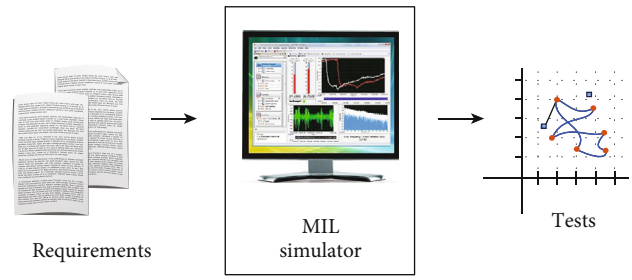

Figure 1: Verification paradigm.

2. Design of Traditional Aircraft Test Systems

Current needs in the design of hardware products in engineering have promoted a new generation of verification or test systems focused on reducing costs and development time. Among these, we highlight the model-based verification methodology [7], which represents the system to be developed by a set of interconnected devices, called Unit Under Test (UUT) (it also frequently appears in the literature as Devices Under Test (DUTs) or Equipment Under Test (EUT)). In this verification methodology, it is possible to define several models with different levels of abstraction [8].

Thanks to this method, different UUTs can be evaluated independently and in parallel allowing, for example, the design of motor control systems without the need of having real motors. This model-based point of view represents an advantage since it permits developing ground tests while considering motors but without having the real device connected to the test system.

The levels of abstraction that are normally considered in model-based verification are the following:

(i) *MIL (Model in the Loop)*. In this approach (Figure 1), all of the UUTs of the system are defined as a general model, obtained according to the specifications. This system can be seen as a type of simulation that enables one to determine whether the complete system meets the required functionality. This way, this model allows capturing the behavior of each UUT, generating with them the stimulus-output pairs to be used in the other levels of abstraction to verify the correct functioning of the system. Generally, these tests are executed in PC-type systems and do not need to be executed in real time

Several authors have focused their researches in this approach, e.g., in [9] where the use of MATLAB/Simulink software to test a model-based fault detection and diagnosis (FDD) for Boeing 747 aircraft is described. In [10], a model-based framework is proposed for wing planform optimization

(ii) *SIL (Software in the Loop)*. At this level, the specifications of the UUT to be tested are replaced by the code that will be implemented by the final device. To perform the verification, the UUT is interconnected to the other models (Figure 2). In this approach, it must be verified that the response of

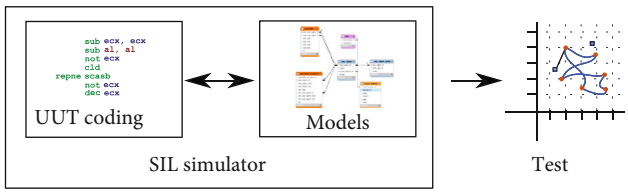

Figure 2: SIL verification paradigm.

the system, using the production code in the UUT, is identical to that obtained in the MIL verification. These checks are generally executed on PC-type systems and do not have to comply with real-time restrictions

Based on this point of view, [11] presents an approach for metamodeling of dynamic systems. The SIL model is used to provide realistic feedback to the test rig, helping to increase the representativeness of the experiment and reducing the costs

(iii) *PIL (Processor in the Loop)*. The production code of the UUT designed in SIL is implemented in a real test unit interconnected to the rest of the system models through appropriate acquisition interfaces (Figure 3). Again, the verification will consist of verifications that the response of this system complies with the specifications, and, consequently, the results are similar to those obtained in the PIL and SIL verifications. This sort of schemes could be used to validate a flight control system. According to this strategy, in [12], the authors propose a system to test the digital implementation of the control system for mini unmanned aerial vehicles (UAVs) based on a low-cost Arduino-embedded microcontroller

(iv) *HIL (Hardware in the Loop)*. This is a verification technique that combines the simulation models of the complete system with a UUT, implemented in real physical hardware (Figure 4). Therefore, in these tests, the UUT to be verified corresponds to a subsystem that is ready to go into production or with a unit already in production in a real system to which one wants to submit tests to verify its correct operating status. In these cases, the UUTs communicate with the acquisition hardware platforms through their Electronic Control Units (ECU)

Therefore, HIL systems are useful both in the initial stages of design and verification and in the maintenance and repair of complete systems in production. In these cases, the concept of CIL (Component in the Loop) systems is used, where the interfaces are connected to the ECU of the system to be monitored and placed inside the complete equipment.

In a HIL/CIL test system, the model of the remaining systems needed for the UUT test is executed on the acquisition hardware platform, complying with the real-time restrictions.

There are many proposals that use this kind of schemes in aviation; e.g., [13] presents a model-based flight control system design approach for a micro aerial vehicle (MAV). This approach uses an integrated flight testing and hardware-in-the-loop (HIL) simulation.

The traceability in these verification systems (Figure 5) is guaranteed by checking that the model of a UUT, at a certain level of abstraction, has a behavior similar to that obtained with its hierarchical superior.

At all levels of abstraction from the PIL level, an acquisition hardware platform is required to interconnect the UUT to the rest of the system models. As a rule, this platform consists of acquisition cards, with appropriate interfaces to communicate to the UUT, connected to a real-time system (real-time computing (RTC)), which is responsible for determining the stimuli that are generated by the acquisition cards and that are recorded and analyzed according to the answers obtained by the UUT. The RTC is also in charge of executing the necessary models to carry out the tests in the HIL/SIL levels.

These HIL/CIL system acquisition hardware platforms are the components that, according to the needs expressed in the introduction, will be developed in this article to increase their standardization, versatility, portability, robustness, modularity, and capacity of interconnection in conducting aviation tests.

In general, the verification systems for the PIL and HIL tests in aviation have a structure that could be described according to what is shown in Figure 6 [14].

The following subsystems are distinguished:

(i) *Operator Panel*. This is the external interface through which it is possible to access the data recorded in the tests or to change the configuration of the systems. Ethernet is usually used as the communication interface

(ii) *Processing Unit*. This is an RTC dedicated to the tasks of acquisition, processing, and generation of the test signals necessary for verification. At the HIL level, it is also responsible for executing the models of the systems to which the UUT is interconnected in the test

(iii) *Instrumentation Bus*. This allows the interconnection of the different acquisition and adaptation systems with the RTC. These are usually specific buses for instrumentation. The most common in aviation are as follows:

(a) *VME (VERSA Module Eurocard)*. This is a modular and real-time system defined for the design of equipment. It was proposed in 1987 by a consortium of companies (Motorola, Mostek, and Signetics, initially). It is widely used in avionics testing platforms, since, being a standard and open system (IEEE 1014 standard, first version defined in 1987 [15]), there are several manufacturers that develop cards for this technology. In these systems, there is a master card that acts as a controller, and working with a series of slave cards, they are responsible for the acquisition and processing of information

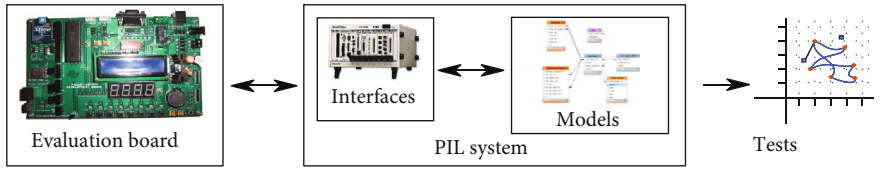

Figure 3: PIL verification paradigm.

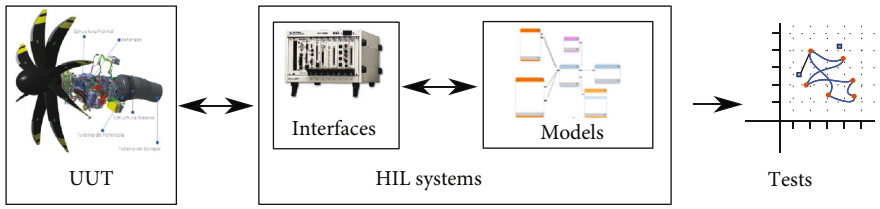

Figure 4: HIL verification paradigm.

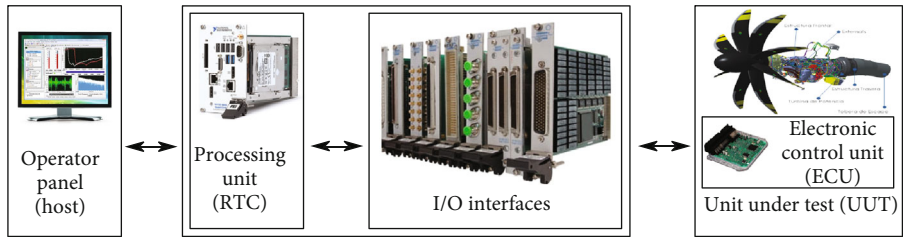

Figure 5: Test equipment.

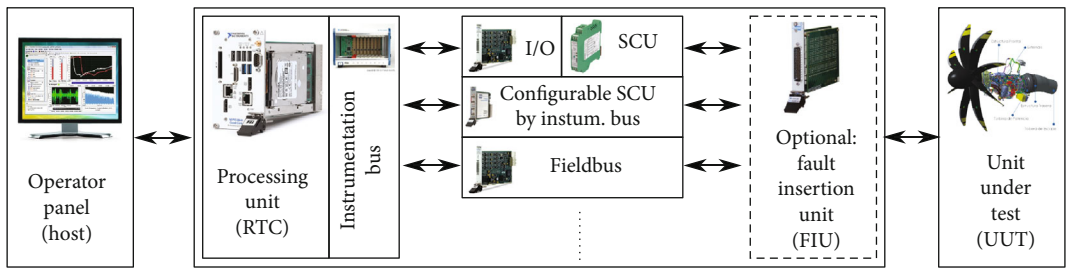

Figure 6: General scheme for avionic verification equipment.

(b) *PXI (PCI eXtension for Instrumentation [16])*. This is an industrial communication bus standard for instrumentation and control. Like VME, it defines modular systems, based on PCI communications, to which synchronization and firing buses have been added, for its use in real-time systems and to guarantee synchronization. It was designed by National Instruments in 1997, and since then, it has become a widely used solution in the industry

(c) *Other Instrumentation Buses*. There are also other solutions, such as NiDAQ, VXS, or VPX, but their use in aviation equipment is less frequent than that in previous ones

(v) *Input/Output (I/O)*. This is the subsystem responsible for acquiring and generating the necessary signals for communication with the UUT. According to their nature, these signals can be an analog value (voltage or current values, within a certain range), a digital value (two discrete values: a high or true value and a low or false one), or a digital communication based on fieldbuses; the following ones are the most common buses in aviation:

(a) *ARINC 429 (Aeronautical Radio, Inc.)*. This is an exclusive standard for avionics systems. This protocol defines a transmission system that describes both the physical layer (based on RS-485 over a twisted pair and interconnections) and the link and upper layers

(b) *AFDX (Avionics Full-Duplex Switched Ethernet)*. This is an Ethernet-based avionics bus defined by Airbus from the ARINC 664 specification, which defines both the physical layer and the communication protocol between an

aircraft's equipment. Its physical layer consists of two twisted pairs, which allows for full-duplex communication and redundancy

(c) *MIL-STD-1553*. This is a standard defined in aviation for the transmission of input/output data by means of a temporal multiplexing of twisted pair data

(d) *CAN (Controller Area Network)*. This is a communication protocol that implements the physical and link levels of the OSI model based on messages with a master-slave topology. Although it is most widely used in automobiles, it is also used in certain avionics systems

(vi) *Signal Conditioning Units (SCUs)*. These are the systems in charge of adapting the signals coming from the aircraft to adequate voltage levels for the input/output cards. Depending on their characteristics, two types of SCU could be distinguished:

(a) *Nonconfigurable*. These SCUs have very high precision, robustness, and linearity. They should be chosen according to the specific application. As a general rule, SCUs of this type comprise complete families, in which the elements are characterized by the specific input and output ranges for which they are designed

(b) *Configurable*. These are less precise than nonconfigurable ones but allow adapting, to some extent, the input and output ranges

The signal conditioning systems are usually either cards designed to measure signals for a specific application or devices designed for a DIN rail. However, there are certain SCUs designed to be connected directly to the instrumentation buses. Most of them are designed for the verification of radio frequency systems

(vii) *Electrical Fault Generator*. This is also called FIU (Fault Insertion Unit) [17] or FIBO (Fault Insertion Break-Out) [18]. This is an optional module required only for the testing of some UUTs, which allows simulating defects in the wiring such as open circuits (cut wires), ground connections, power connections, and pin-to-pin connections (a short circuit between wires)

Although this structure is quite general, each UUT requires different input modules in different quantities. Thus, for example, the test of a certain UUT may require a CAN connection [19] and not require analog signals, while another may not require connecting to any fieldbus, but multiple analog inputs/outputs may be needed. Therefore, this UUT would therefore need completely different verification equipment. In addition, depending on the UUT, each I/O may require a different adaptation. So, not only do the number and type of I/O modules change but also the number and type of SCUs change, as well as the wiring of them with the I/O modules.

For this reason, the great complexity and heterogeneity of the different UUTs of an aircraft have traditionally led to the development of a hardware acquisition platform for the verification of each UUT per aircraft type (or even for each system to be tested within the same UUT). Consequently, the designed tests have generally been carried out by manual procedures. Although these procedures allow the development of robust test systems with good connectivity, they do not meet the requirements of standardization, versatility, modularity, and size desired in this research, since they are, as a rule, neither portable equipment nor easily reconfigurable for the realization of various tests. In addition, having different test devices increases significantly the cost of the ground test equipment [20].

This problem is not unique to the aviation sector. It also appears frequently in other sectors such as automotive industry or in industrial automation. Therefore, various solutions have been proposed in the design of more flexible verification equipment. In order to design a platform that best fits the specified requirements, a detailed analysis of these solutions is carried out in the following section. As it will be seen, all of these solutions are based on modifying the general structure depicted in Figure 6 and generally add devices that either are reconfigurable or enable the modification of the interconnections between the I/O, SCU, and ECU modules of the UUT in each test.

3. Portable and Configurable Ground Test System for the A400M Aircraft

To verify the requirements that the acquisition hardware of the test verification system must meet, it is necessary to know the number of signals that the system should be able to control simultaneously. In order to fulfil this aim, a signal analysis on the aircraft simulation database has been carried out with the purpose of determining the number of inputs and outputs that are needed simultaneously on every test execution over the aircraft under study (A400M).

In this analysis, a data collection of simultaneous executions was carried out.

Figures 7 and 8 depict a summary of this analysis. Every graph shows the number of signals used in the ground test simultaneously. Four different test stations have been considered, denoted as SC2 (light blue), SD1 (red), SE1 (dark blue), and SG1 (green). As it can be observed, there is great dispersion of the number of signals used in every test. In this sense, it is possible to identify a probability distribution described by a mean (red line) and a standard deviation that best describes the flexibility that the test equipment must have.

Therefore, it has been possible to specify which constraints are required by the system of acquisition of the ground verification system. To fully execute all of the ground tests, the system has had to simultaneously control over 57 analog input signals, 48 analog output signals, 202 digital input signals, and 162 digital output signals.

Considering the special requirements of the aviation sector, technological solutions based on HIL/CIL verification

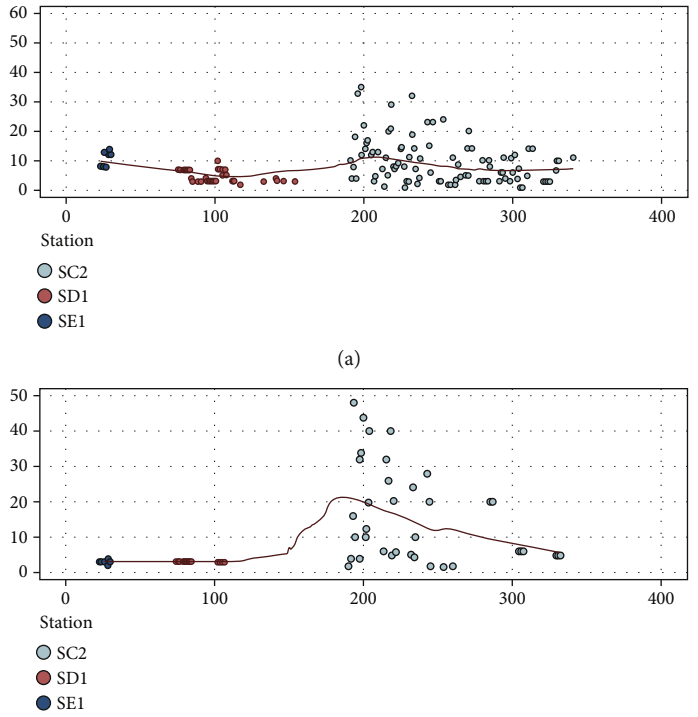

Figure 7: Analog signal analysis (simulated data) used in different ground verification test orders for this project. Number of signals (y-axis) vs. test order (x-axis): (a) inputs and (b) outputs.

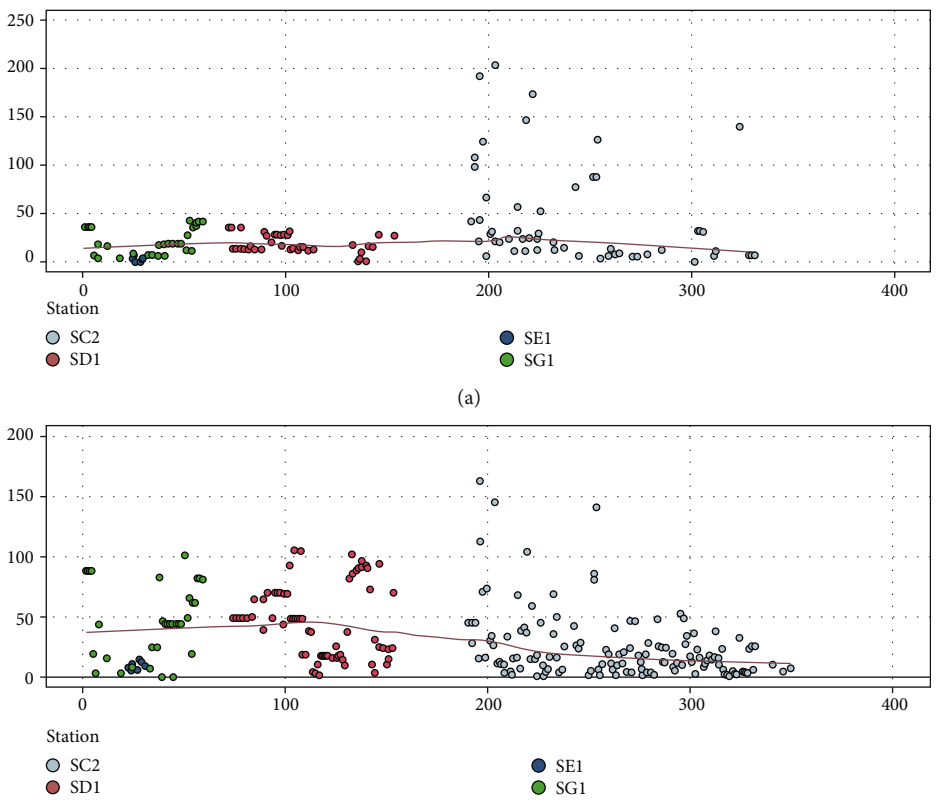

Figure 8: Digital signal analysis (simulated data) used in different ground verification test orders for this project. Number of signals (y-axis) vs. test order (x-axis): (a) digital inputs and (b) digital outputs.

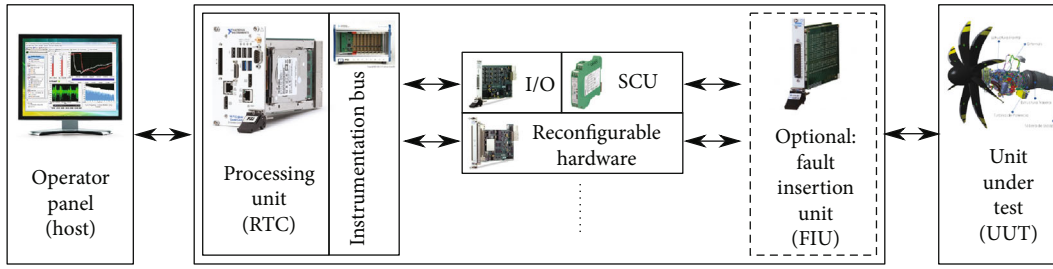

Figure 9: Verification equipment with reconfigurable hardware.

equipment are the most suitable. In this sense, three approaches could be considered. The following sections describe each of them.

3.1. Systems Based on Reconfigurable Hardware. The most common reprogrammable hardware used in verification equipment is based on the use of FPGAs (Field-Programmable Gate Arrays). Verification equipment using this approach implements an architecture such as the one shown in Figure 9.

These systems take advantage of their feature to reconfigure the FPGA hardware for the design of I/O systems and have the possibility to control and convert signals at a low level. This allows the system, on the one hand, to reduce to a certain extent the capacity of the required SCUs and, on the other hand, to integrate, in a single configurable device, multiple systems of interconnection to several fieldbuses without requiring additional modules.

If, for example, the verification equipment requires an ANRIC 429 bus controller, instead of using a specific I/O card, an FPGA and its GPIOs can be used. From a functional point of view, once the FPGA is programmed, it can be seen as another module that handles all of the tasks related to the medium access (demodulation, management of the lower layers of the communication protocols, etc.). This is very similar to how a specific card would act. It is even possible to implement microprocessors inside the FPGA, which makes them highly flexible systems [21].

FPGAs have generic output ports that can read and write at high speeds. Therefore, these ports can be used both as direct discrete signals and for the implementation of fieldbus controllers or system emulation, although they will generally require an external SCU, since an FPGA usually works with very low voltage levels. For this reason, the use of FPGA has been proposed for the design of various HIL/SIL verification equipment.

Its use has also been proposed for the design of flexible aviation test equipment, which can be seen in the following researches:

(i) In [22, 23], the authors propose a system based on a combined use of FPGAs and the RTC for the realization of verification equipment based on models. To do this, the authors propose the use of FPGAs for the design of control modules for aviation fieldbuses in a way that reduces the need to buy multiple adapters. However, it is necessary to keep in mind that each subsystem added to an FPGA consumes certain resources (memory, LUT (Lookup Table) units, etc.), so there is a maximum limit of subsystems that can be implemented on these devices

To solve this, the authors propose generating catalogs of solutions for each subsystem, each typified by their characteristics (fundamentally, FPGA resource requirements and necessary execution time) so that the system will automatically choose the optimal implementations of each subsystem, depending on the requirements demanded by each test and on the number of subsystems to be implemented

The proposed solution has been successfully tested for the design of CIL verification equipment for the Eurocopter helicopters of the Airbus company, demonstrating that this technology allows increasing the flexibility of avionic verification systems

(ii) In [24], the authors propose HIL verification equipment for autopilot tests in unmanned aircraft or UAVs. This hybrid verification equipment allows for the checking and tuning of the control parameters of these devices

For the design of the HIL system, the authors have opted for the design of a system that integrates the following modules:

(a) *FPGA*. This is used for the processing of digital input/output signals and for implementing the necessary fieldbus controllers of the application

(b) *DSP (Digital Signal Processor)*. This is in charge of performing flight control and of processing analog signals

The proposed system and the code of the verification tests, developed with LabVIEW, have been tested with a simulation, showing that the platform, despite being economic, is very flexible and allows us to develop, in a fast way, different tests on the system.

This great versatility means that modules with FPGAs can easily be found on the market for their connection to the most instrumentation buses used in verification equipment.

Although these FPGAs can solve problems of adaptations of digital signals, to be used in the processing of analog signals, they require either external ADCs (Analog-to-Digital

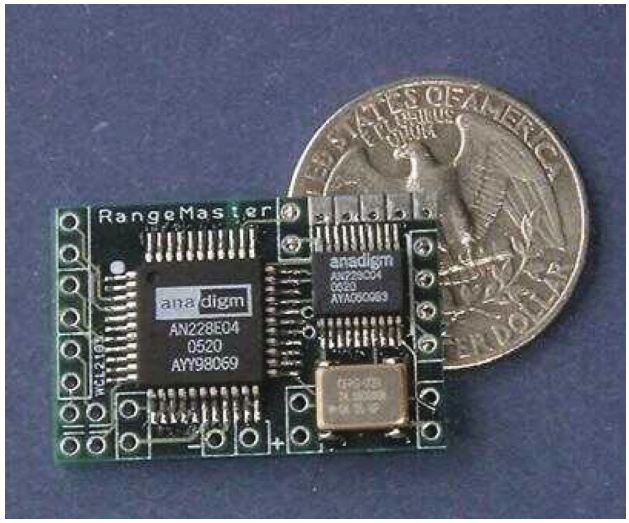

Figure 10: Anadigm FPAA evaluation module.

Converters) or the use of FPGAs with analogical interfaces AFE (Analog Front Ends), which are present in a few commercial models.

In these devices, it is possible to perform complete signal processing since the AFE provides some analog processing capacity, while the FPGA allows for the synthesis of digital filters or demodulators. Although it could be an appropriate technology, there are currently no commercial I/O modules for instrumentation buses that use this type of FPGA.

Furthermore, there is a growing tendency nowadays to research in the design of reconfigurable analog systems, such as the FPAA (Field-Programmable Analog Array), an analog counterpart of the FPGAs, where the digital blocks have been replaced by analog units formed by operational amplifiers and passive components so that the interconnections of these complex analog circuits can be implemented with adders, integrators, filters, etc. In any case, at the present time, there are few commercial solutions that implement this technology, beyond the devices offered by Anadigm [25] or Lattice [26] (Figure 10).

In conclusion, reconfigurable hardware modules have a series of advantages, which are explained as follows:

(i) Increasing the flexibility of the system, especially for the treatment of digital signals

(ii) Reducing dependency on I/O modules, above all, for the management of fieldbuses

(iii) A higher accessibility, as there are modules with FPGA for most of the current instrumentation buses

However, they also have the following disadvantages, which must be taken into account depending on the application to be developed:

(i) They require SCUs. In general, they still depend on certain external electronics to adapt the levels of the input signals to the thresholds admitted by the reprogrammable electronic modules

(ii) They are not designed for analog signal processing. Although there are technological solutions for the processing of these signals using reconfigurable hardware, they are not widespread or are in the research phase

(iii) The cost is higher. Although prices have become considerably cheaper, reconfigurable hardware is still generally expensive

(iv) Development times are initially increased. The increase in flexibility using these devices comes from their reprogramming capacity, but this also has the disadvantage that it is necessary to have software modules for each of the functionalities to be implemented. For example, if an ARINC bus interface is needed, it is first necessary to have the code of this module duly verified. Thanks to the reusability presented by these modules, this increase only occurs if the modules have not been previously developed for another test or aircraft

(v) They require an inventory of needs for each test. Within an FPGA, multiple modules can be loaded, which would work in parallel for the management of the different signals to be treated, but each of them uses certain resources to be managed. Depending on the requirements of each module, some tests are not feasible because they require more resources than available

(vi) They require specific training requirements. It is important to keep in mind that although there are alternatives for synthesizing FPGAs that use common programming languages such as C, they are not very efficient, and it is recommended to use more task-specific languages such as VHDL or Verilog, which require the use of trained personnel in these areas

3.2. Systems Based on Industrial Solutions. Because the amount of I/O ports required in automation strongly impacts the cost of the facilities, various solutions have been developed to increase the number of inputs and outputs available without needing to buy additional modules.

In the following sections, a description of these industrial solutions is provided while considering those best matching the requirements in aviation.

3.2.1. Multiplexors. A multiplexer is an electronic device that allows for the redirecting information from various sources to a destination. Its symbolic representation and simplified operating scheme are represented in Figure 11.

As it can be seen in the figure, a multiplexer has the following ports:

(i) *Inputs*. These are information channels, usually from the process to be verified, of which one will be connected to the output

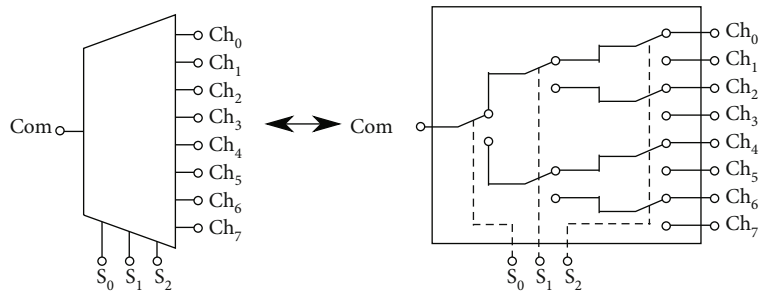

Figure 11: Multiplexed verification equipment.

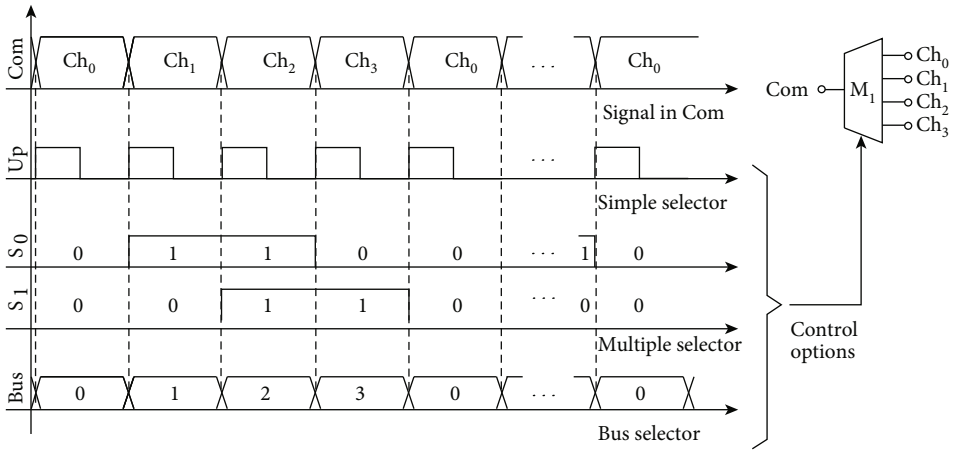

Figure 12: Types of selection signals.

(ii) *Output*. This is also called the common terminal. It will be electrically connected to an input, depending on the selection

(iii) *Ports for Control or Selection*. These are the input signals that allow the channel to be redirected to the output. There are multiple types of selection inputs, and the most common are shown in Figure 12:

(a) *Up/Down*. This is suitable for sequencing. They switch for each signal pulse by increasing (up) or decreasing (down) a channel in the selection. This selection method is specifically designed to carry out sequencing, which consists of reading all of the channels by multiplexing in time. They usually have an additional input to select channel 0 directly (to reset the input)

(b) *Discrete Selection Signals*. The input channel to be selected is encoded with several input pins through a natural binary number, allowing for direct switching between all of the input channels. They allow for the sequential reading of channels

(c) *Bus*. The channel to choose is sent by a bus, generally an industrial one, although recently, new multiplexers have also been developed that allow for the selection using a USB port

From a generic point of view, a multiplexer can be understood as a set of switches that are connected and disconnected depending on the selection inputs. Therefore, its characteristics are strongly conditioned by the technology used for the design of the multiplexers. The most common ones are the following:

(i) *Relays*: These are electromechanical devices whose functionality is similar to that of controlled switches. These devices activate a set of contacts that allow for the opening or closing of one or several independent electric circuits. They have the advantage of being robust elements, capable of working with high voltages and currents, but the closing of the circuits requires a certain mechanical movement. This movement causes the relays to have lifetimes limited by a number of commutations and with a high switching time. Therefore, they are not an adequate technology for reading by sequencing. They tend to be of two types:

(a) *Electromagnetic*. In these relays, the contact closure is caused by the electromagnetic attraction generated by a coil. They are usually adequate to handle high powers, but they are very bulky

(b) *Reed*. These use contacts formed by thin sheets of metal that are joined together in the presence of a magnetic field. While the power that they can handle is more limited than that in the electromechanical case, their switching is somewhat

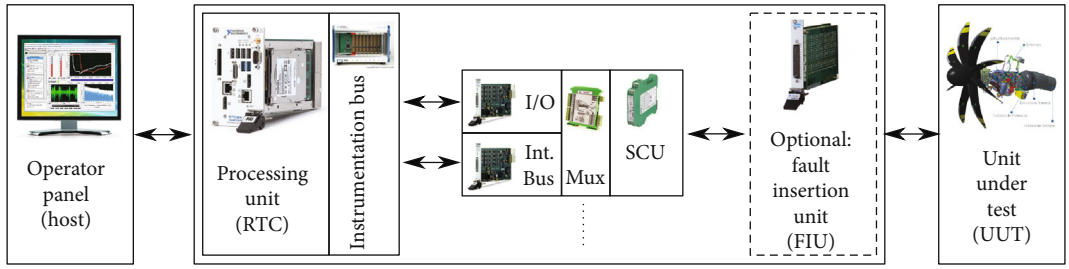

Figure 13: Multiplexed verification equipment.

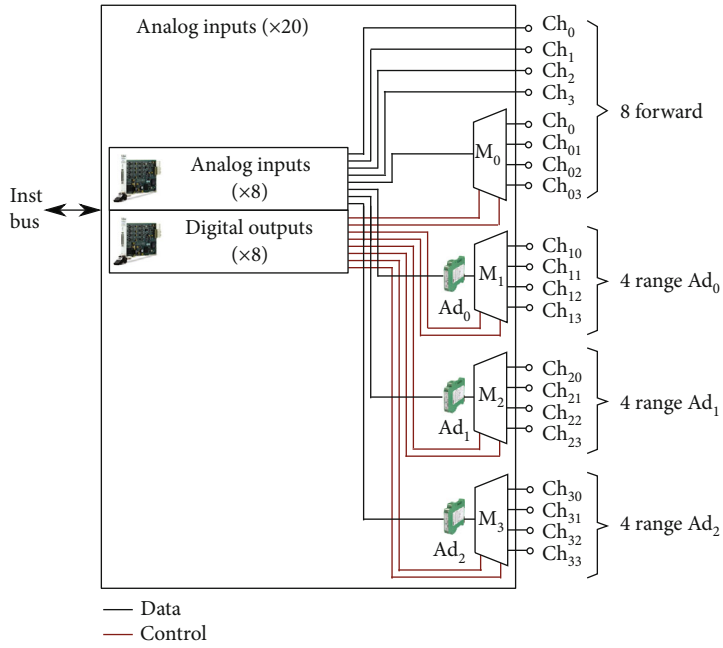

Figure 14: Example of use.

faster. Furthermore, they have very small sizes. Like in the electromagnetic type, the lifetime of reed relays is determined by a maximum number of commutations

(ii) *An Integrated Design using Transistors, Generally Field Effect Transistors (FET)*. These transistors behave like switches by generating an electric field through a control pin called gate. They have the advantage of being very fast, having a theoretically unlimited number of commutations, and being of small size, thus allowing for reading by sequencing. However, due to thermal dissipation reasons, the power that can be controlled is usually more limited than that in electromagnetic ones, because, in conduction, the transistors introduce small resistance that generates losses in the form of heat. Depending on the manufacturing technology, this conduction channel can be bidirectional (allows for the circulation of current in both directions) or unidirectional

In the case of verification systems, as shown in Figure 13, the implementation of this technology allows for reducing the number of necessary input signals (basically analog, although they can also be used with digital signals), either by sequencing or selection, while optimizing the use of resources such as SCUs.

For our verification system, placing the multiplexers after the input channels could be proposed, either with or without the SCU, thus following a connection scheme similar to that described in the example of Figure 14.

As it can be observed in this case, the multiplexers of the example allow us to extend 8 analog input channels for up to a total of 20 signals:

(i) 8 direct channels (4 of them multiplexed with the possibility of reading after sequencing)

(ii) 4 multiplexed with the Ad_0 adaptation

(iii) 4 multiplexed with the Ad_1 adaptation

(iv) 4 multiplexed with the Ad_2 adaptation

In this example, we have opted for the use of digital selection inputs, which requires 8 signals. In conclusion, reconfigurable hardware modules have a series of advantages, which are explained as follows:

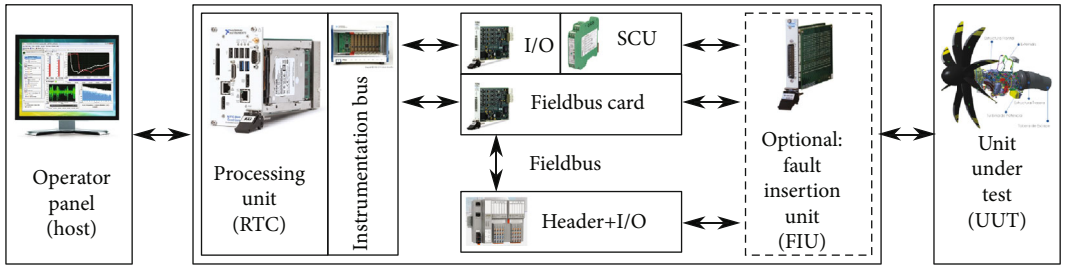

Figure 15: Verification equipment with headers.

(i) They increase the flexibility of the system and allow for a software reconfiguration of the verification system

(ii) They reduce the number of I/O modules, especially in the case of analog inputs, although they can also be used for digital signals

(iii) They have a lower cost, as multiplexers are significantly cheaper than the I/O modules that they replace

(iv) They are more robust, as it is an industrial solution commonly used in automation systems

With respect to the drawbacks for the application to be developed, the following ones should be highlighted:

(i) Reconfigurable hardware modules are designed to work with industrial levels. Certain signal levels used in aviation do not coincide with those commonly used for automation. In these cases, the use of additional SCUs to adapt the levels is necessary

(ii) They have limited redirection capabilities. The multiplexers are intended to, in principle, redirect a series of input signals to a digital analog converter, but the degree of reconfiguration flexibility required for the verification equipment may cause greater required routing flexibility. In these cases, it is preferable to use technologies such as switching matrices (see Section 3.3), which are more flexible, allowing us to also emulate the behavior of multiplexers

3.2.2. DCS Headers. Communication headers are a widely used solution in industrial automation, and they arise from the automation model DCS (Distributed Control System), which reduces wiring costs through the use of fieldbuses. With this technology, all elements of the installation become elements within a network that share information between themselves.

In these facilities, the headers are autonomous control equipment that allow for the managing of multiple inputs and outputs, both analog and digital. This equipment is designed to minimize the costs of wiring in extensive installations, since they allow placing the headers and, therefore, the necessary inputs and outputs, close to the equipment to be controlled.

The headers are independent PLC (Programmable Logic Controller) systems, which are deterministic and that are designed for real-time operations, with communications through an industrial bus. They could be configured with various modules that incorporate the input or output ports required by the application. That is, the inputs and outputs to be arranged in each header are configurable based on adding the appropriate modules to the equipment.

Normally, the manufacturers have a complete line of headers, all of them with similar characteristics, but they could change the industrial bus to which they can be connected, with Ethernet, Modbus, or CAN headers being the most usual ones.

In a generic scheme, its use for verification equipment is detailed in Figure 15.

As it can be seen, these headers allow for reducing the number of I/O modules based on connecting various inputs to them. Although this architecture does not reduce the complexity of the system, it is necessary to consider that the cost of the modules for DCS headers is cheaper than that for the architectures based on instrumentation buses.

As an example, Figure 16 shows a scheme with 24 analog inputs, 8 analog outputs, and 64 digital outputs divided into two headers connected to the same fieldbus. Although a single header could handle this periphery, it may be advisable either to reduce wiring costs or to increase reliability and to distribute the inputs and outputs in multiple headers on the same bus, since each one of them is a unit that acts independently, communicating directly with the RTC.

In addition, the use of multiple headers allows for increasing the rate of data acquisition, which is usually related to the average data rate used in this type of devices communicated by industrial fieldbuses.

The main advantages of DCS headers are summarized as follows:

(i) They increase the flexibility of the system. Each DCS header acts as an autonomous real-time system with its own self-management and programming capabilities. Therefore, the failure in one module does not affect the other equipment in the system

(ii) They reduce the number of I/O modules, especially in the case of analog inputs, although they can also be used for digital signals

(iii) The DCS headers are cheaper than the I/O modules for industrial buses they replace

(iv) They have heterogeneous signals: each header can handle multiple inputs and outputs, both digital and analog

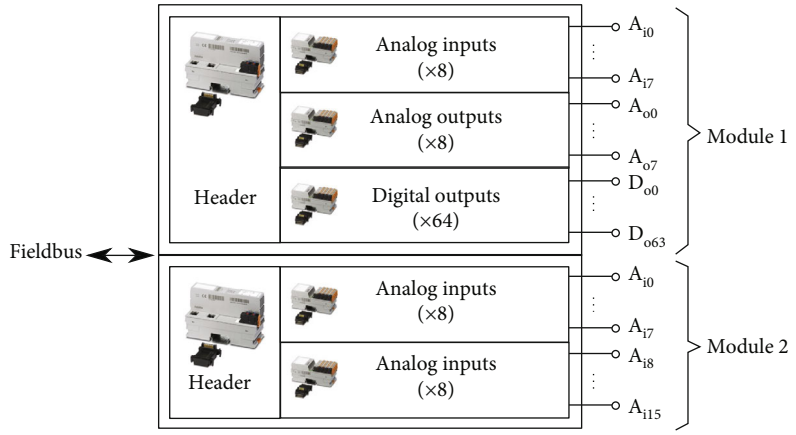

Figure 16: Example of use.

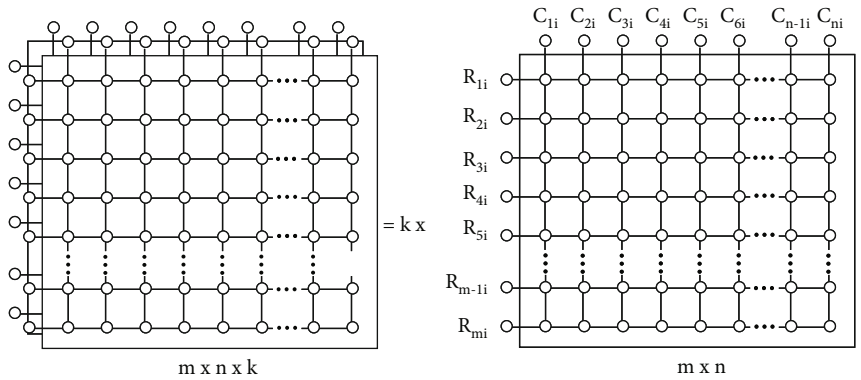

Figure 17: Internal structure of a connection matrix.

(v) They are usually very compact modular devices, facilitating the design of small equipment

(vi) They are robust, since it is an industrial solution commonly used in automation systems

Their main drawbacks are the following:

(i) They are designed to work with industrial levels. Similar to the case with multiplexers, they constitute equipment designed for automation applications, so certain aviation signals are outside their operating range

(ii) They have limited bandwidth. The need to establish communications between the RTC and the DCS headers reduces the effective sampling rate of the system. This effect can be alleviated in part thanks to their programming capacity and their autonomy if a registration policy is used in buffers and with the appropriate temporary tables. For example, instead of reading a single piece of information, a number of signals recorded during a certain period of time are read in the communications

(iii) They have a specific programming structure and languages. In many cases, the programming is based on the IEC 61131 standard, which is common for the programming of industrial PLCs, but not very frequent in aviation. Therefore, additional training for the verification test development teams may be required

3.3. Systems Based on Switching Matrices. In the field of HIL or CIL systems, the need to redirect signals between different devices is very common. Although in cases of low complexity, this can be solved with multiplexers, there are certain applications in which a capacity of total connection between different elements is required, which can be solved with matrix switchers.

These matrices consist of an ordered arrangement of rows, columns, and layers of switches, as shown in Figure 17.

In these structures, there are switches arranged in all intersections between rows and columns, so that, if a switch is closed, all of the layers are closed, in a way similar to how all the independent circuits of a relay are closed. The most common is usually a one-layer or two-layer matrix. The latter is especially indicated for cases that need to redirect bipolar signals.

Technologically, these matrices use switches similar to those used for multiplexers, but the need to have a higher degree of connection requires the use of systems that are compact. Therefore, the most used solutions are those based on reed relays or FET.

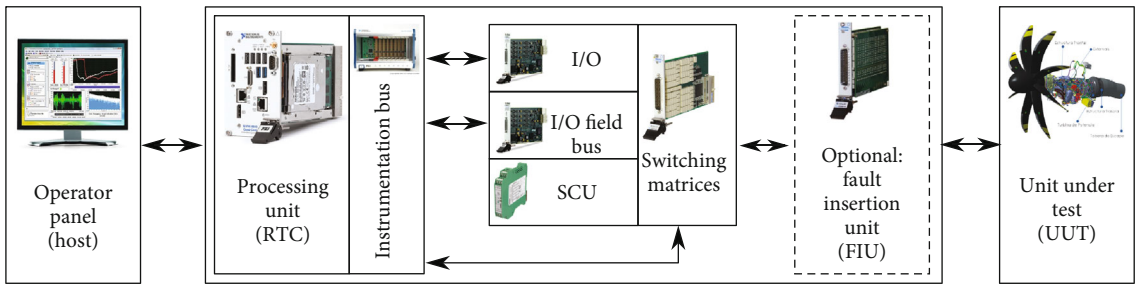

Figure 18: Verification equipment with a commutation matrix.

In addition, as with multiplexers, in the case of systems using reed relays, their lifetimes are limited by the number of commutations. Therefore, manufacturers usually have mechanisms to allow for the replacement of them in case of failure.

According to what it has being seen, the interconnection capacity of the matrices depends on their number of connections (rows, columns, and layers). Therefore, their name is given in terms of these parameters. For example, a $32 \times 8 \times 2$ matrix will have two layers, 32 rows, and 8 columns. Bearing in mind that all of the connections in the matrices are usually externalized, we will understand that the card will thus have a connector with more than 512 pins (in the case of the example). In addition, by means of suitable wiring, several of these cards can be combined to increase the sizes of the matrices.

These characteristics make them suitable to increase the flexibility of the HIL/CIL verification systems.

Next, several technological solutions will be proposed that rely on this technology for the design of reconfigurable test systems, as required in the objectives of this research.

3.3.1. Discrete SCUs. As shown in Figure 18, the matrices are used in the verification equipment to connect I/O modules and fieldbuses in a flexible manner depending on the test to be performed.

This configuration allows the HIL/CIL verification equipment to make the following modifications to adapt to the needs of the test to be performed:

(i) *Previous Configuration*. The matrices allow us to connect the specific UUT signals required to the I/O modules and the SCU before beginning a test, thus optimizing the available resources

(ii) *Hot Configuration*. These systems also enable the modification of the interconnection of the signals during the experiments. Thanks to this, it is possible to reduce the number of I/O ports of the HIL/CIL equipment, since it is not necessary to dimension the systems to the signals required by each test, but only to those that are required simultaneously. This allows reducing the size and increasing the modularity and functionality of the verification equipment

(iii) *Emulation of Multiplexers*. The large routing capacity offered by the matrices allows them to be used to perform the same operations indicated for the multiplexers, such as sequencing reading, as long as the technology of the chosen switches allows it

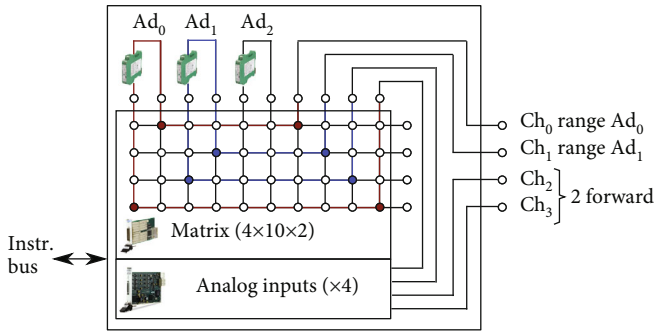

Figure 19: Example of using a matrix with a discrete SCU.

Figure 19 shows an example of verification equipment with a switching matrix and discrete SCUs. In this case, there is a system with 4 analog inputs, which can be reconfigured during the course of the test to act directly on different channels of the UUT or through one of the SCUs (Ad_0 to Ad_2) of the equipment. If more than one channel is required to use the same SCU simultaneously, it could be shared by sequencing.

In the example of the figure, the system has been wired to have two direct channels (Ch_2 and Ch_3), one channel using the Ad_0 converter (Ch_0) and one using the Ad_1 (Ch_1), leaving the Ad_2 unused in this case.

Therefore, to summarize, the switching matrices have the following advantages:

(i) They increase the flexibility of the system through the reconfiguration of the routing of the UUT signals and the SCUs towards the I/O modules

(ii) They reduce the number of I/O modules. Thanks to the capacity of hot reconfiguration, they can dimension the systems to the signals that are actually used simultaneously instead of those required by the test. In the case where FET matrices are used, sequencing would allow us to further reduce the number of input channels required

However, they also present the following drawbacks:

(i) *Cost*. While they are very flexible systems, they are also expensive

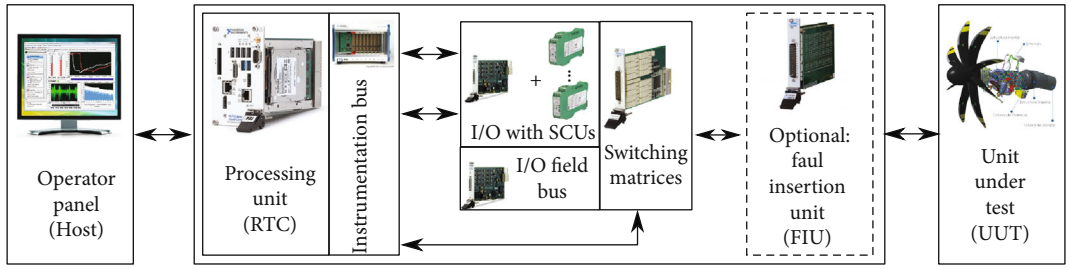

Figure 20: Integrated HIL verification equipment.

(ii) *Limited Lifetime*. In the case of using reed technologies, the switches have a lifetime that depends on the number of commutations

(iii) *Ability to Generate Failures*. Due to their great flexibility, the operators that design the tests must be especially careful not to generate transients that cause failures in the systems, such as short circuits. This is especially problematic when using the utilities offered by the manufacturers for the use of these matrices that were not used to consider automatically this effect

3.3.2. Integrated HIL Systems. Integrated HIL systems are understood as solutions offered by different manufacturers that seek to integrate configurable I/O SCU modules by bus instrumentation and matrix switchers to increase the flexibility of the systems.

These solutions have an architecture like the one shown in Figure 20.

In these systems, each input channel has a configurable SCU, designed according to the final application, generally in automobiles. However, the equipment with these characteristics could be adapted to the verification equipment in aviation.

To summarize, these solutions have the following advantages:

(i) *Flexibility*. Since they are equipment developed to perform various verification tests for aviation, they fulfill the requirements of the research

Their most important disadvantages are the following:

(i) *Solutions in the Development Phase*. There are few manufacturers with commercial solutions designed with these characteristics, so their availability is not guaranteed in the market, and, in many cases, manufacturers still do not offer complete documentation or sale prices

(ii) *Limited Portability*. Most of the solutions presented here correspond to COTS (Commercial Off-The-Shelf) systems designed for fixed installations

(iii) *Cost*. In the case of the presented COTS solutions, the manufacturer has estimated the common needs that their clients may require. This is an estimation that does not always coincide with the reality. Therefore, in these solutions that are sold as closed equipment and final solutions, it is likely that certain components could be purchased unnecessarily for our particular application. This effect increases the final cost

4. Discussion

Initially, it can be assumed that there is no generic solution for the hardware/software design of the architecture of the test equipment that best matches all of the sets of ground tests, especially considering the Airbus A400M aircraft. However, in order to select the best approach, the following stages in ground verification tests must be considered:

(i) At an initial design stage, high flexibility in the definition of number and types of signals is needed: analog, digital, voltage and intensity ranges, etc.

(ii) At a verification stage, real interconnections with the UUT are convenient in order to match the requirements as closer to reality as possible. In a model-based scheme, the uncertainties of the model could derive in significant errors that could be important in the in-flight performance of the aircraft

(iii) At maintenance and repairing stages of the complete verification system, it could be necessary to replace, to readapt, or to increase the number of interconnections

(iv) The tests to be developed could be required to be executed in real time (RTC)

Based on these considerations, the best approach should be based on HIL/CIL systems.

According to this approach, it is estimated that the most appropriate solution for the addressed problem is a hybrid configurable verification test system that can consider the different solutions presented in this paper. In this sense, the main contribution of the paper can be synthesized in a methodology to design ground test equipment focused on the specified requirements (size and portability, robustness, modularity, connectivity, standardization, versatility, and ease of configuration). Therefore, our proposal suggests the following methodology based on the four steps:

(i) First, the configuration of the AIM must consider the use of DCS headers in those cases where signals

require high flexibility of voltage and intensity range and high data acquisition rate

(ii) Second, the number of switching matrices has to be estimated according to the desired scalability. The use of this component enables the increase in the effective number of signals of the I/O modules (with sequencing where possible) and the signal routing flexibility among the DUT, the SCUs, and I/O modules

(iii) Third, to increase the flexibility of the system, the use of reconfigurable and modular SCUs has to be dimensioned in order to enhance the flexibility of the ground test equipment hardware

(iv) Fourth, the final design should also take into account the costs and supply capacity of the manufacturers for the design of the final system, especially in the case of using very novel solutions or recent appearance in the market

5. Conclusions

The study developed in this paper has considered several approaches for developing a new generation of ground testing equipment with the aim of meeting the requirements specified in modern aviation. These requirements include portability, flexibility, and configurability for the AIMs that connect to the aircraft. The described work has been carried out in cooperation with the Airbus DS Company, and it has been focused specifically on the A400M aircraft.

A conceptual review of traditional design in aircraft test systems has been developed. The results of this analysis have allowed us to identify the necessity of an abstraction methodology in ground test systems. This strategy implies the need of implementing appropriate hardware platforms that best perform the interconnection among the UUT and the rest of the system models. These platforms are constituted by customized electronic components (acquisition cards, routing devices, signal conditioning units, etc.) that can perform real-time computing, being responsible for generating the stimuli for every test and being responsible for registering the answers of the UUT.

During the execution of the project, several real ground tests over the Airbus A400M aircraft have been carried out. This analysis has allowed us to determine the number and type of signals that are needed during ground tests. Based on the obtained results, we have been able to propose the use of a HIL/CIL approach for the verification ground test platform because they are appropriate both in the initial stages of design and verification and in the maintenance and repair of complete systems. Furthermore, they can develop tests in real time (RTC).

Airbus has taken into account the above recommendations for the proposal of new ground test equipment. Following the methodology proposed in this paper, Airbus is currently designing a new prototype for the next generation of AIMs in the A400M aircraft. The synthetized methodology has been proven to meet the specified requirements. Due to the confidentiality agreement, the authors cannot give further details about the obtained results.

Data Availability

No data were used to support this study.

Conflicts of Interest

The authors declare that they have no conflicts of interest.

Acknowledgments

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