A DIRECT SYNTHESIS METHOD OF CASCADED CONTINUOUS-TIME SIGMA-DELTA MODULATORS

Ramón Tortosa, José M. de la Rosa, Angel Rodríguez-Vázquez and Francisco V. Fernández

Instituto de Microelectrónica de Sevilla – IMSE-CNM (CSIC)
Edificio CICA-CNM, Avda. Reina Mercedes s/n, 41012- Sevilla, SPAIN
Phone: +34 95 5056666, Fax: +34 95 5056686, E-mail: {tortosa|jrosa|angel|pacov}@imse.cnm.es

ABSTRACT

This paper presents an efficient method to synthesize cascaded sigma-delta modulators implemented with continuous-time circuits. It is based on the direct synthesis of the whole cascaded architecture in the continuous-time domain instead of using a discrete-to-continuous time transformation as has been done in previous approaches. In addition to place the zeroes of the loop filter in an optimum way, the proposed methodology leads to more efficient architectures in terms of circuitry complexity, power consumption and robustness with respect to circuit non-idealities.[†1]

1. INTRODUCTION

Continuous-Time (CT) Sigma-Delta Modulators (ΣΔMs) have demonstrated to be an attractive solution for the implementation of Analog-to-Digital (A/D) interfaces in systems-on-chip integrated in deep-submicron standard CMOS technologies [1]. Although most reported ΣΔMs have been implemented using Discrete-Time (DT) circuits, the increasing demand for broadband data communication systems has motivated the use of CT techniques. In addition to show an intrinsic antialiasing filtering, CT ΣΔMs provide potentially faster operation with lower power consumption than their DT counterparts [2][3].

In spite of their mentioned advantages, CT ΣΔMs are more sensitive than DT ΣΔMs to some circuit errors, namely: clock jitter, excess loop delay and technology parameter variations [2][3]. The latter are specially critical for the realization of cascaded architectures. This has forced the use of single-loop topologies in most reported silicon prototypes even thought low oversampling ratios (<12) are needed [4][5], whereas very few cascaded CT ΣΔM Integrated Circuits (ICs) have been reported [6].

However, the need to achieve medium-high resolutions (>12bits) within high signal bandwidths (>20MHz) while guaranteeing stability, has prompted the interest in proper methods for the synthesis of high-order cascaded CT ΣΔMs [7]-[9]. These methods are based on applying a DT-to-CT transformation to an equivalent DT topology that fulfils the required specifications. In most cases, the use of such a transformation is normally translated into an increase of the analog circuit complexity with the subsequent penalty in silicon area, power consumption and sensitivity to parameter tolerances.

†1. This work has been supported by the Spanish Ministry of Science and Education (with support from the European Regional Development Fund) under contract TEC2004-01752/MIC.

This paper presents a direct synthesis method of cascaded CT ΣΔMs which, dispensing with the DT-to-CT equivalence, allows to reduce the number of analog components and to efficiently place the zeroes/poles of the noise transfer function, thus yielding to more robust architectures than using a DT-to-CT transformation.

2. CASCADED CT ΣΔ MODULATORS

Fig.1 shows the conceptual block diagram of a m-stage cascaded CT ΣΔM. Each stage, consisting of a single-quantizer CT ΣΔM, re-modulates a signal containing the quantization error generated in the previous stage. Once in the digital domain, the outputs, y_i, of the stages are properly processed and combined (by the cancellation logic) in order to cancel out the quantization errors of all the stages, but the last one in the cascade. This latter error appears at the overall modulator output shaped by a function of order equal to the summation of the order of all the stages.

Cascaded CT ΣΔMs are normally synthesized from equivalent (well-known) DT systems and use the same digital cancellation logic [8]. This DT/CT equivalence can be guaranteed because the overall open loop transfer function of each stage in Fig.1 is in fact a DT system [2]. Thus, in the case of a rectangular impulsive response of the Digital-to-Analog Converter (DAC), it can be shown that the equivalent DT loop filter

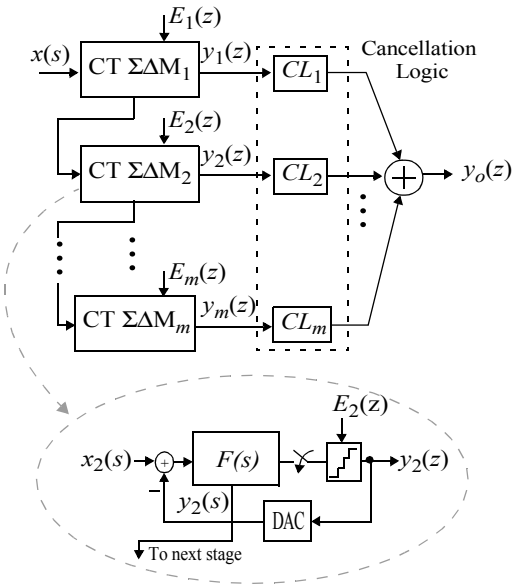

Figure 1. Conceptual block diagram of a cascaded CT ΣΔM.

transfer function is given by [10][11]:

$$F(z) = \sum_{p_i} \mathrm{Re}\left(\frac{F(s)}{s} \cdot \frac{e^{m_1 T_S \cdot s}}{z - e^{T_S \cdot s}} \right) - \sum_{p_i} \mathrm{Re}\left(\frac{F(s)}{s} \cdot \frac{e^{m_2 T_S \cdot s}}{z - e^{T_S \cdot s}} \right) \quad (1)$$

where $f_s = 1/T_s$ is the sampling frequency; $m_1 = 1 - t_d/T_s$; $m_2 = 1 - (t_d + \tau)/T_s$; t_d and τ are respectively the time delay and pulse width of the DAC waveform; p_i are the poles of $F(s)/s$ and $\mathrm{Re}(x)$ stands for the residue of x.

However, in order to get a functional CT ΣΔM while keeping the cancellation logic of the original DT ΣΔM, every state variable and DAC output must be connected to the integrator input of later stages [8], thus increasing the number of analog components, i.e transconductors, amplifiers and DACs. As an illustration, Fig.2(a) shows a cascaded 2-1-1 CT ΣΔM obtained from an existing DT ΣΔM [12]. Note that at least eight scaling coefficients (k_{g2-9}) and their corresponding signal paths are needed to connect the different stages of the modulator. The number of integrating paths can be reduced – as illustrated in Fig.2(b) – if the whole cascaded ΣΔM is directly synthesized in the CT domain as proposed in the next section.

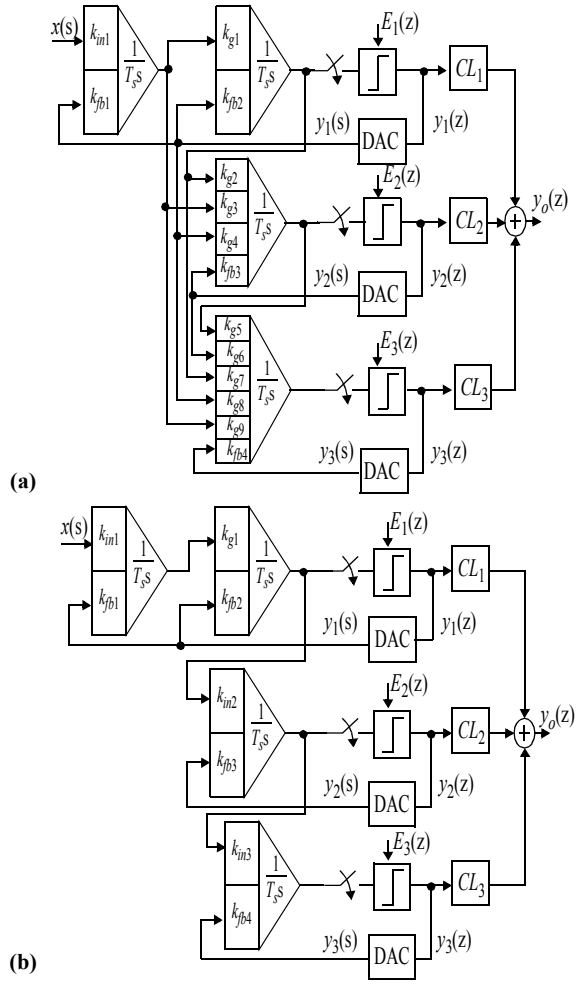

Figure 2. Cascaded 2-1-1 CT ΣΔM architecture obtained (a) from an equivalent DT ΣΔM (b) using the proposed method.

3. PROPOSED METHODOLOGY

The idea of dispensing with the DT-to-CT transformation was previously reported in [3] for single-loop architectures. However, in the case of cascaded architectures, the cancellation logic functions (not present in single-loop ΣΔMs) must be included in the synthesis procedure in order to get an optimum architecture.

Let's consider the more general case of the m-stage cascaded CT ΣΔM shown in Fig.1. The overall output, y_o, is given by:

$$y_o(z) = \sum_{k=1}^{m} y_k(z) CL_k(z) \quad (2)$$

where $y_k(z)$ and $CL_k(z)$ represent respectively the output and partial cancellation logic transfer function of the k-th stage.

If the modulator input, $x(t)$, is set to zero, it can be shown that the output of each stage can be written as:

$$y_k(z) = \frac{E_k(z) + \sum_{i=1}^{k-1} Z\left\{ L^{-1}[H_D F_{ik}]\big|_{nT_s} \right\} y_i(z)}{1 - Z\left\{ L^{-1}[H_D F_{kk}]\big|_{nT_s} \right\}} \quad (3)$$

where Z stands for the Z-transform, L^{-1} is the inverse Laplace transform, $H_D \equiv H_{DAC}(s)$ is the transfer function of the DAC, and

$$F_{ij} \equiv F_{ij}(s) = \frac{\text{Input Quantizer j}}{y_i(s)} \quad (4)$$

represents the transfer function from $y_i(s)$ to the input of j-th quantizer.

Using the notation $Z\left(L^{-1}(H_D F_{km})\big|_{nT_s} \right) \equiv Z_{km}$, the output of each stage is given by:

$$y_k(z) = \frac{E_k(z) + \sum_{i=1}^{k-1} Z_{ik} y_i(z)}{1 - Z_{kk}} \quad (5)$$

and the output of the modulator can be written as:

$$y_o = \sum_{k=1}^{m} y_k CL_k = \sum_{k=1}^{m} \left(\frac{E_k}{1 - Z_{kk}} + \frac{1}{1 - Z_{kk}} \sum_{i=1}^{k-1} Z_{ik} y_i \right) CL_k \quad (6)$$

The partial cancellation logic transfer functions can be calculated by imposing the cancellation of the transfer function of the first $m-1$ quantization errors $E_k(z)$ in (6). This gives:

$$CL_k(z) = \frac{-Z_{km} CL_m}{1 - Z_{mm}} = \frac{-Z\left\{ L^{-1}[H_D F_{km}]\big|_{nT_s} \right\} CL_m(z)}{1 - Z\left\{ L^{-1}[H_D F_{mm}]\big|_{nT_s} \right\}} \quad (7)$$

where the partial cancellation logic transfer function of the last stage, $CL_m(z)$, can be chosen to be the simplest form that preserves the required noise shaping.

It is important to mention that the design equations (2)-(7) do not only take into account the single-stage loop filter transfer functions (F_{ii}), but also the inter-stage loop filter transfer functions ($F_{ij}, i \neq j$). The latter are continuous-time integrating paths appearing only when the modulator stages are connected to form the cascaded ΣΔM and must be included in the synthesis methodology to obtain a functional modulator with minimum number of inter-stage paths.

Therefore, the following procedure can be used in a systematic methodology for the synthesis of cascaded CT ΣΔMs[†2]:

- First, the poles of different transfer functions ($F_{ij}(s)$) are optimally placed in the signal bandwidth for given specifications. Scaling is needed in order to optimize the dynamic range of each integrator. This process is carried out entirely in the CT domain and no equivalence to an existing DT modulator needs to be imposed.
- Second, once the individual stages are designed and optimized, cancellation logics are calculated using (7).

4. SYNTHESIS EXAMPLE

For illustrative purposes, the 2-1-1 CT ΣΔM of Fig.2(b) is synthesized using (2)-(7) to achieve 16-bit resolution in a 750 kHz bandwidth, with a sampling frequency of 48MHz (oversampling ratio, $M = 32$) [12]. Although in the proposed methodology the modulator in Fig.2(b) would be entirely designed in the CT domain, a slightly different approach will be used in this particular case in order to facilitate the comparison of the performance of both modulators in Fig.2. The coefficients of the first stage ($k_{in1}, k_{g1}, k_{fb1}, k_{fb2}$) are taken to be equal in both systems and are obtained from a DT-to-CT transformation of the first stage of a DT ΣΔM in [12]. The rest of coefficients in Fig.2(b) are taken such that the time constant of the integrators is the inverse of the sampling frequency:

$$\begin{aligned} k_{in1} &= -k_{fb1} = 1/4; \qquad k_{fb2} = -3/8 \\ k_{g1} &= k_{in2} = -k_{fb3} = k_{in3} = -k_{fb4} = 1 \end{aligned} \tag{8}$$

Hence, the single-loop and inter-stage transfer functions are given by:

$$\begin{aligned} F_{13} &= \frac{(sT_s k_{fb2} + k_{fb1}) k_{in2} k_{in3}}{(sT_s)^4} \\ F_{23} &= \frac{k_{fb3} k_{in3}}{(sT_s)^2} \\ F_{33} &= \frac{k_{fb4}}{sT_s} \end{aligned} \tag{9}$$

and the partial cancellation logic transfer functions can be calculated using (7). This gives:

$$\begin{aligned} CL_1 &= \frac{-Z\left\{L^{-1}[H_D F_{13}]\big|_{nT_s}\right\}}{\left(1 - Z\left\{L^{-1}[H_D F_{33}]\big|_{nT_s}\right\}\right)} CL_3 \\ CL_2 &= \frac{-Z\left\{L^{-1}[H_D F_{23}]\big|_{nT_s}\right\}}{\left(1 - Z\left\{L^{-1}[H_D F_{33}]\big|_{nT_s}\right\}\right)} CL_3 \end{aligned} \tag{10}$$

From (8)-(10) and using a Non-Return-to-Zero (NRZ) DAC, the following cancellation logics are derived:

$$\begin{aligned} CL_1 &= \frac{z^{-1}}{48}(7 + 29z^{-1} - 7z^{-2} - 5z^{-3}) \\ CL_2 &= z^{-1}(1 + z^{-1})(1 - z^{-1})^2 \\ CL_3 &= 2(1 - z^{-1})^3 \end{aligned} \tag{11}$$

where CL_3 is chosen to have three zeroes at DC, corresponding to the zeroes contributed by the first three integrators.

In order to verify the proposed methodology, both modulators in Fig.2 were simulated using SIMSIDES, a SIMULINK-based time-domain behavioral simulator for ΣΔMs [13]. Fig.3 shows two ideal output spectra of the modulators

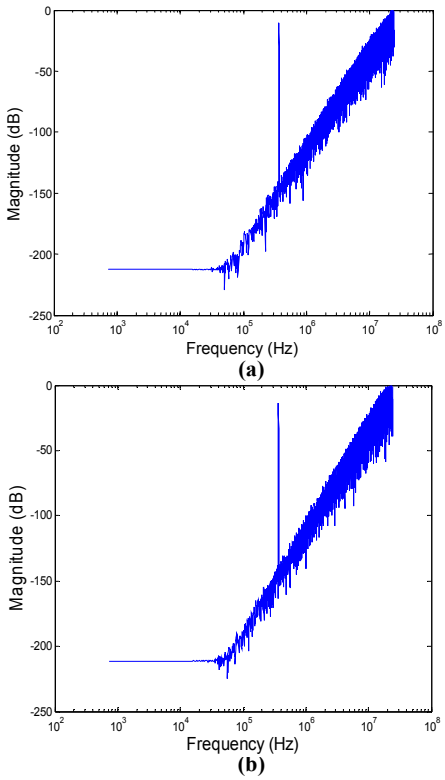

Figure 3. Output spectrum of a cascaded 2-1-1 CT ΣΔM obtained from: (a) an equivalent DT ΣΔM; (b) the proposed synthesis method.

†2. In this procedure, the modulator order, oversampling ratio and number of bits of internal quantizers are assumed to be determined for given specifications from well-known expressions [1].

showing a similar performance. The effect of mismatch on the Signal-to-Noise Ratio (SNR) was also simulated. For this purpose, maximum values of mismatch were estimated for a 0.18 µm CMOS technology and both modulators in Fig.2 were simulated considering a Gm-C implementation. The results are shown in Fig.4, where the SNR loss is represented as a function of the standard deviation of the transconductances (σ_{gm}) and capacitances (σ_C). For each point of these surfaces, 150 simulations were carried out using random variations with the standard deviation given in the diagrams. The value of SNR loss represented in Fig.4 stands for the difference between the ideal SNR, i.e with no parameter variation, and the SNR with 90% of the 150 simulations above it. It is shown that the lower analog component count in Fig.2(b) is reflected in a lower variance of the modulator coefficients, leading to a better behaviour in terms of sensitivity to mismatch.

The same reasoning can be applied to the requirements in terms of DC gain of the individual transconductors. Since the number of transconductors connected to the same node is higher in the previous method, the equivalent impedance associated with these nodes tends to be lower and the requirements in terms of the individual transconductor output impedance is higher. Therefore, a higher DC gain is needed. Fig.5 illustrates this point. Note that the SNR-peak starts dropping at a DC gain $\cong 8$dB higher in the case of the system designed following the previous method.

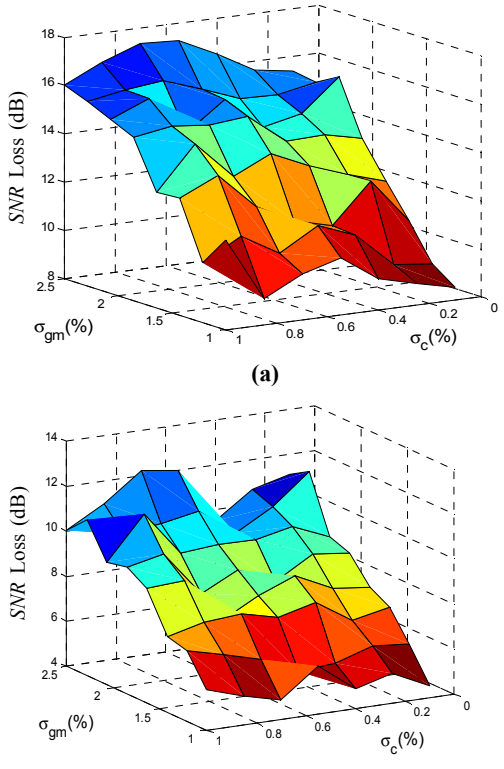

Figure 4. Effect of mismatch on the SNR of a cascaded 2-1-1 CT ΣΔM obtained from: (a) an equivalent DT ΣΔM; (b) proposed method.

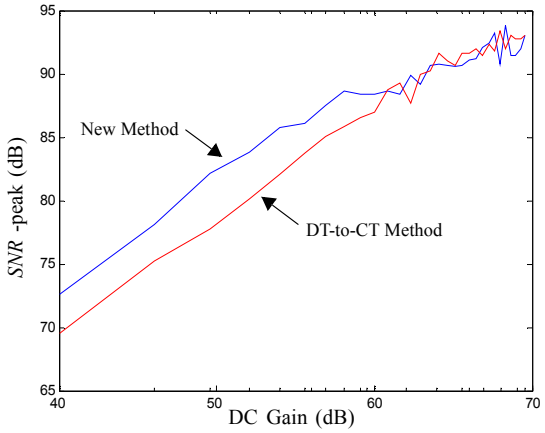

Figure 5. Effect of DC gain on the SNR-peak.

CONCLUSIONS

In this paper a new methodology of synthesizing cascaded continuous-time ΣΔ modulators has been presented. It is demonstrated that more efficient topologies in terms of circuit complexity can be generated if the design is directly done in the continuous-time domain and the cancellation logic transfer function is taken into account in the synthesis procedure. Behavioral simulations considering critical error mechanisms validate the presented approach.

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