Design and Electrical Implementation of a 1.8-V Multistandard Switched-Current ΣΔ Modulator

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***Abstract*— This paper describes the design and electrical implementation of a 1.8-V, 0.18μm CMOS reconfigurable switched-current ΣΔ modulator for multistandard (Bluetooth, WCDMA) communication systems. The modulator topology is an expandible cascade architecture which can be reconfigured both at the architecture level and at the circuit level in order to adapt the modulator performance to the different standards with adjustable power consumption. For this purpose, programmable Class AB memory-cell arrays are used to implement the modulator loop filter. Simulation results are shown that demonstrate correct operation for all standards, featuring 11bits dynamic range within 1MHz and 7.8bits within 3.8MHz bandwidth.**

I. INTRODUCTION

IN addition to the actual diving forces of the IC industry, we are witnessing an unprecedented development of wireless communications, introducing a large number of new applications and standards into the market. These new standards –such as Bluetooth, IEEE 802.11 and UMTS– are complementing rather than replacing the existing ones – like for instance GSM. This trend demands integrated low-cost, smaller and faster multistandard radio transceivers that can be reconfigured to operate over a variety of specifications in order to take advantage of the different services offered by co-existing wireless technologies [1]. Moreover, it is desirable for those transceivers to be able to process broadband wireline standards, thus making it possible the wireless/wireline convergence in portable multipurpose devices. The common radio receiver architecture is the so-called superheterodyne. To date, wireless implementations use the architecture invented by E. Amstrong in 1918 with minimum variations. In practice the main drawback of that architecture is the analog components variations. That is the reason why analog circuitry is minimized in order to process more signals in digital domain. Here, the Analog-to-Digital Converter (ADC) is one of the most challenging building blocks in multistandard receivers because of the different sampling rates and dynamic ranges required to digitize the wide range of signals coming from each individual operation mode. One of the most important design challenges consist in handling these signals with little adjustment made to circuit parameters and adaptive power consumption [2]. Sigma-Delta Modulators (ΣΔMs) are good candidates for the implementation of the ADC in multistandard communication systems. This type of ADCs combines redundant temporal data (*oversampling*) to reduce the quantization noise and filtering (*noise shaping*) to push this noise out of the signal band. On the one hand, the use of these characteristics results in high-performance, robust ADCs, which have lower sensitivity to circuitry imperfections than Nyquist-rate ADCs, thus making easier to include reconfigurability and programmability functions without significant performance degradation. On the other hand, ΣΔMs trade analog accuracy by signal processing, thus facilitating their integration in modern deep-submicron VLSI technologies [3].

Although most reported ΣΔMs have been implemented using *switched-capacitor* (SC) circuit techniques, the need to achieve high-performance in adverse low-voltage, digital-oriented CMOS processes, has motivated exploring analog design techniques compatible with those technologies. This is the case of the *switched-current* (SI) technique, which during the last decade has been used to implement ADCs for digital communication chips [4], [5]. In addition to its obvious compatibility with digital technologies (only MOS transistors are used), the SI technique offers several advantages. Some of them are the following:

- As signal carriers are currents, the signal range is not limited by supply voltage, thus being suited to low-voltage operation.
- SI basic building blocks, called memory cells, are based on current mirrors [5]. This fact makes SI circuits relatively easy to be programmed and reconfigured for different specifications.

Thus SI circuits constitute a suitable design technique for multistandard applications.

This paper presents the design and electrical implementation of a fully differential SI ΣΔM in a 1.8-V, 0.18μm CMOS technology. The modulator topology is a reconfigurable cascade architecture, which has been designed to cope with two different standards: Bluetooth and WCDMA. The main building block is a Class AB memory cell which can be digitally programmed to adapt the modulator performance to each standard with adaptive power consumption. Transistor level simulations of the whole SI ΣΔ modulator are shown, demonstrating a correct operation in a 1MHz bandwidth with 11bits dynamic range and 7.8bits within 3.8MHz bandwidth. These figures locate this circuit on a competitive position within of the state-of-the-art SI ΣΔ modulators.

II. PROGRAMMABLE SWITCHED-CURRENT ΣΔ MODULATOR

A. *Reconfigurable architecture*

Figure 1 shows a MASH ΣΔM architecture which is a good candidate to fulfill all the requirements imposed by different communication standards. It could be implemented in different ways by combining single-loop (stable) first-order and second-order modulators, using both single and multibit internal quantization [3].

In our case, a reconfigurable architecture is required in order to adapt the modulator performance to the different standard specifications. Figure 2 shows a 2-1^P expandable version of the cascade architecture of Fig. 1, made up of a second-order first-stage followed by P first-order stages which are connected or disconnected according to the required noise-shaping. In addition, analog and digital coefficients are optimized according to the criteria described in [3]-[6].

Using a linear model for the internal quantizers, it can be shown that the Signal-to-Noise Ratio (*SNR*) of the modulator in Fig. 2 can be written as [3]:

$$SNR = 10\log\frac{P_s}{P_q} \qquad (1)$$

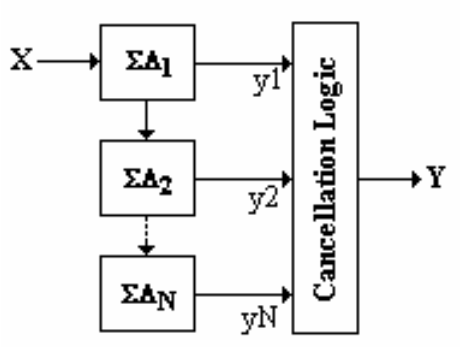


Figure 1. MASH ΣΔ modulator.

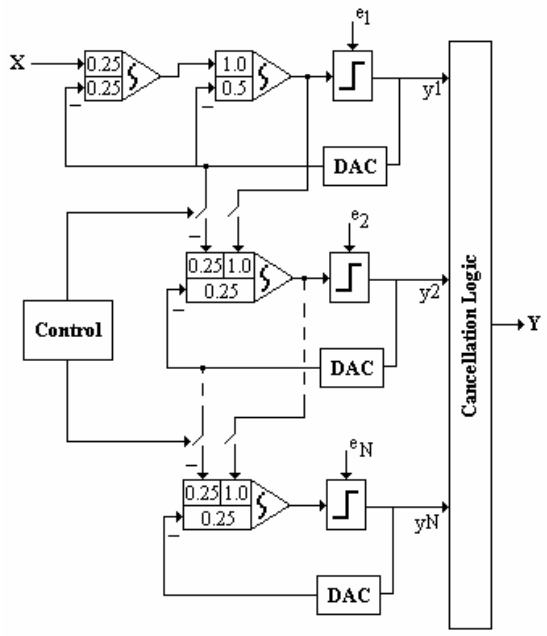


Figure 2. Reconfigurable 2-1^P ΣΔ modulator.

where $P_s = \frac{m^2 I_{ref}^2}{2}$, $P_q = \frac{4(2Iref)^2 p^{2*N}}{12(2N+1)M^{2N+1}}$, N is the modulator's order, M is the oversampling ratio, I_{ref} is the DAC referent current and m is the ratio between input signal and I_{ref}, often referenced as modulation index.

Figure 3 shows the *SNR* vs. *M* for different modulator orders. It can be noted that different performances can be achieved by varying the modulator order, i.e, the number of stages of the modulator in Fig. 2.

B. *Programmable switched current memory cell*

In addition to reconfigure the modulator architecture as described in previous section, the basic building blocks that compose the modulator, i.e, the memory cells, can be also reconfigured in order to achieve the required modulator specifications with adaptative power dissipation. For this purpose, the programmable SI memory cell shown in figure 4 is proposed.

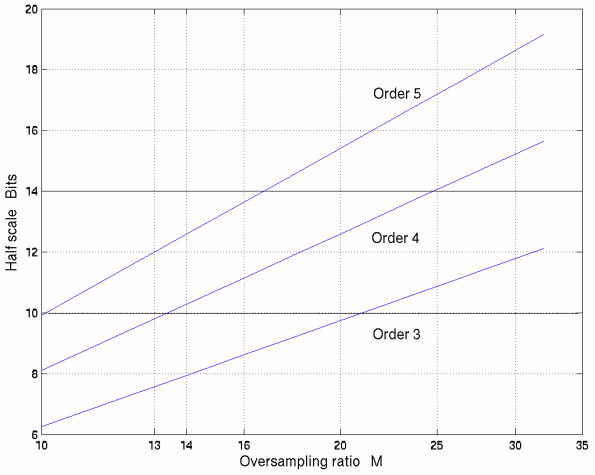


Figure 3. *SNR* vs oversampling ratio.

Assuming that the thermal noise is the dominant source of error, the *SNR* of a unitary memory cell is given by [5],

$$SNR = 10\log\frac{m_o^2 I_{bias}^2}{\left(S_{nT} + \frac{tg_{m1}}{4C_{gs}}S_{nT}\right)BW_s} \quad (2)$$

where $S_{nT} = \frac{8}{3} m_{th} KTg_{m1}$, m_{th} is a process's constant, K is the boltzmann's constant, T is the temperature, g_{m1} is the memory transistor's transconductance, g_{ds} is the output conductance of the memory transistor, I_{bias} is the bias current, C_{gs} is the gate-source capacitance, t is the clock signal on-time and BW_s is the signal bandwidth. If L cells are connected, the *SNR* of the whole memory cell is given by:

$$SNR = 10\log\frac{m_o^2 L^2 I_{bias}^2}{L\left(S_{nT} + \frac{tg_{m1}}{4C_{gs}}S_{nT}\right)BW_s} \quad (3)$$

which after some mathematical manipulation can be written as:

$$SNR = SNR_{unitary} + 10\log(L) \quad (4)$$

which improves in 10log(L) with respect to the case of a unitary memory cell. Regarding other SI errors apart from thermal noise, the performance of the unitary cell is basically the same as that of the whole cell. The rationale behind this is that most SI errors can be expressed as a ratio between two electrical parameters (g_{m1}, g_{ds}, c_{gs}) [5], which can be generically expressed as:

$$e = \frac{f(g_{ds}, g_{m1})}{f(g_{m1}, C_{gs})} \quad (5)$$

As these parameters are equally modified by a L factor when L cells are connected together, the resulting error of the whole cell is the same as that of the unitary cell.

The performance of SI ΣΔMs has a great dependence on the *SNR* of the integrators. Among the others, the most limiting factors are due to the front-end integrator. It can be shown that the SNR of a SI ΣΔ modulator can be written as [7]:

$$SNR = 10\log\frac{P_s}{P_q + P_{nI}} \quad (6)$$

where P_q is the in-band quantization noise power and P_{nI} is the in-band thermal noise power of the front-end integrator, given by:

$$P_{nI} = \left(\frac{t}{T_s} + \frac{t^2}{T_s}\frac{g_{m1}}{4C_{gs}}\right)\left(\frac{16}{3} m_{th} KTg_{m1} BW_s\right) \quad (7)$$

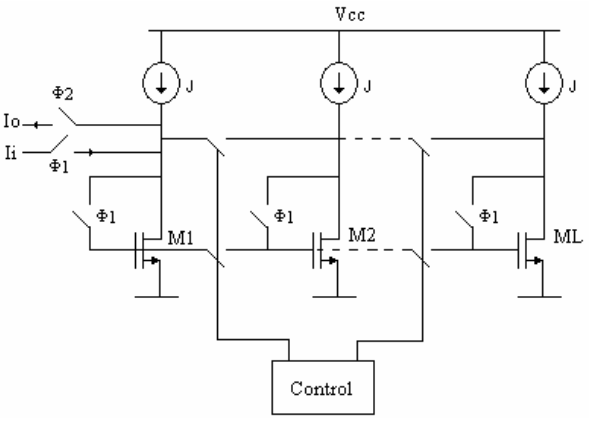
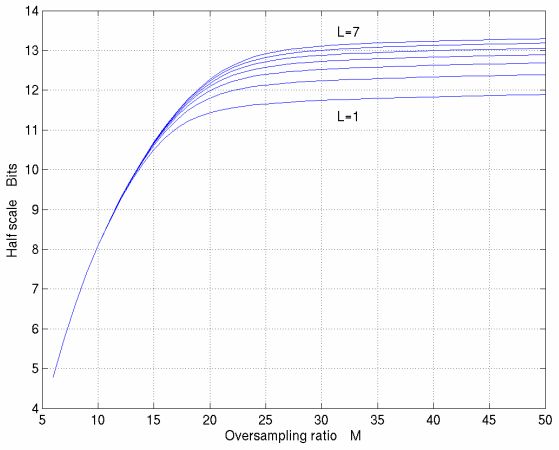
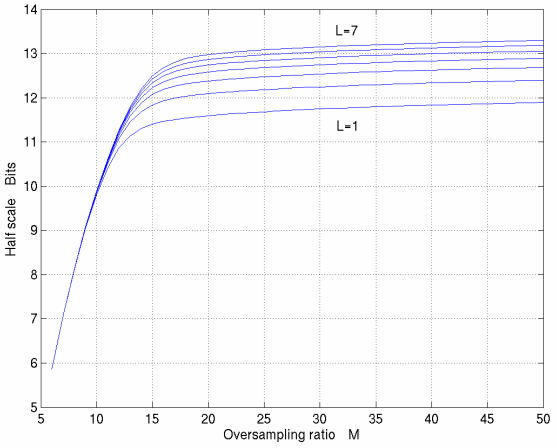


Figure 4. Programmable SI memory cell.

Therefore, by using a SI integrator based on programmable SI memory cells, the *SNR* of the modulator can be increased according to (4), which is true if the modulator is designed in such a way that the thermal noise power be the dominant source of error. As an illustration, figure 5 shows how the *SNR* of 2-1^P SI ΣΔ modulators can be improved by increasing the number of unitary cells which are connected in the programmable-based SI integrator.



a) 2-1^2 Modulator and BW$_s$=1MHz (Bluetooth)



b) 2-1^3 Modulator and BW_s=3.8MHz (WCDMA)

Figure 5. *SNR* versus *M* for different SI ΣΔ modulators.

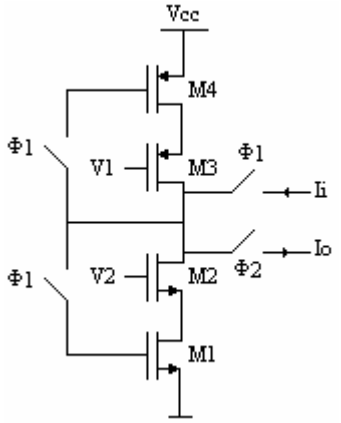


Figure 6. Class AB memory cell.

In this case, a unitary class AB memory cell like that shown in figure 6 was considered, with a bias current of 500uA and circuit errors lower than 0.1%. This cell is suitable for low-voltage applications like in this paper, because it can operate at high sampling frequencies, while keeping low values of SI errors and power consumption [8,9].

Note from figure 5 that different specifications required in some communication applications can be achieved by properly selecting the modulator order, the oversampling ratio and the number of memory cells used in the programmable integrator, as detailed in the next section.

III. A CASE STUDY

As a case study, a reconfigurable SI ΣΔ modulator has been designed in a 1.8-V, 0.18μm CMOS technology to cope with the following specifications:

- Bluetooth: 11-bit resolution within a 1MHz
- WCDMA: 8-bit resolution within a 3.8MHz

A. *Architecture selection*

The above requirements can be achieved by different combinations of modulator order, oversampling ratio (sampling frequency) and number of unitary cells. Table 1 shows a summary of some of these combinations. Among them, the 2-1 and $2\text{-}1^3$ modulators have been selected for the bluetooth and WCDMA, respectively. These architectures have been selected because they achieve the best trade-off between power consumption (related to the sampling frequency) and silicon area (related to the number of memory cells).

Table 1. Candidate SI ΣΔ modulator architectures

11Bits @ 1MHz				8Bits @ 3.8MHz		
Order *N*	#Cell *L*	Fs MHz		Order *N*	#Cell *L*	Fs MHz
2-1	***3***	***70.4***		2-1	2	136.8
$2\text{-}1^2$	2	40.0		$2\text{-}1^2$	2	91.2
$2\text{-}1^3$	2	26		***$2\text{-}1^3$***	***2***	***70.4***

Table 2. Basic block specifications

	Bluetooth	WCDMA
Integrator		
I_{bias}	1.5mA	1.0mA
ε_s	0.1%	0.1%
ε_g	0.1%	0.1%
ε_q	0.1%	0.1%
g_m	6m	4m
C_{gs}	3.9pF	2.6pF
Switch-on resistance	<100Ω	<100Ω
Comparator		
Resolution time	<3ns	<3ns
Hysteresis	<60uA	<60uA
DAC		
Resolution	1 bit	1 bit
Reference	600uA	600uA

B. *Design of the main building blocks*

One of the most important blocks in SI ΣΔ modulators is the integrator. The main design considerations for this block are the signal swing, the SI errors and the sampling frequency. For this case study, a fully differential Forward Euler integrator was designed using the class AB memory cell shown in figure 6. Cascode transistors, extrinsic gate to sourse capacitors and CMOS-dummy switches were used in order to reduce all SI errors below 0.1%. The integrator is designed to cope with a programmable signal swing from 1 to 1.5mA which is required for the modulator, considering the different standards. As an illustration, figure 7 depites the transient response of the integrator for a sinusoidal input of 400μA and frequency 5MHz, showing a correct operation.

Another important building block is the one-bit quantizer (comparator). Figure 8 shows the selected topology, consisting of a regenerative latch and a RS flip-flop [11,12]. One of the most important limiting factors of this circuit is the mismatch error, wich is controled with the sizing of the reset switch and also by right layout. HSPICE simulations show 1ns resolution time and 55μA hysteresis, which agree with the specifications shown in Table 2. As an illustration, figure 9 shows the step response of the comparator for an input signal of ±200μA.

Finally, figure 10 shows the schematic of the one-bit DAC. It is made up of two current sources controlled by the quantizer output. This block was designed to provide the required reference current without degrading the output-input conductance ratio error of the integrators which were 0.08% and 0.07% to the output positive and negative, respectively.

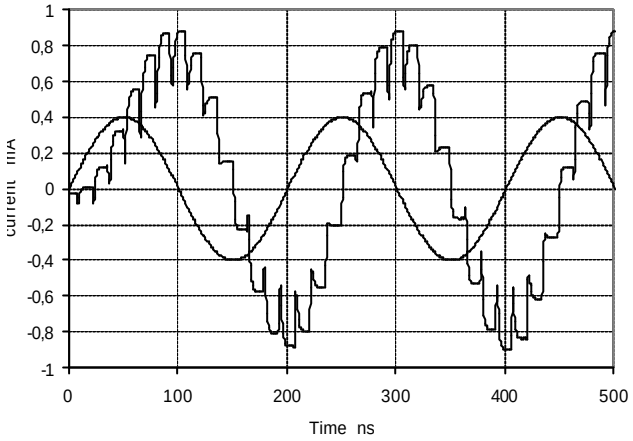


Figure 7. Transient response of the SI integrator in HSPICE.

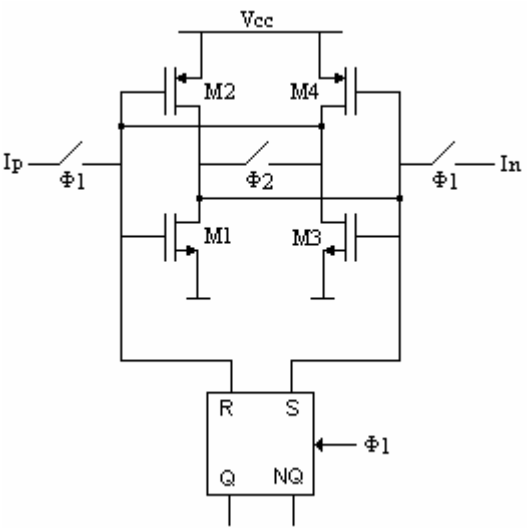


Figure 8. Comparator.

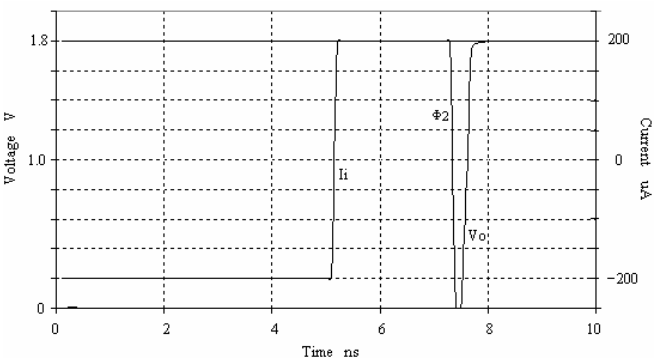


Figure 9. Transient response of the comparator.

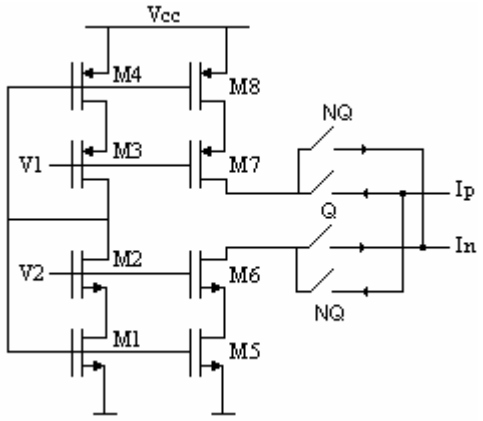


Figure 10. DAC.

IV. SIMULATION RESULTS

In order to evaluate the performance of the reconfigurable SI ΣΔ modulator described in the previous section, time-domain full transistor simulations using HSPICE were done. As an illustration, figure 11 shows the output spectra of the modulator for the different operation modes, i.e. Bluetooth and WCDMA, considering a half-scale input sinewave signal at 410kHz. The effective resolution is 11bits for Bluetooth and 7.8bits for WCDMA. This is better illustrated in figure 12, where the *SNR* is plotted versus the relative input amplitude.

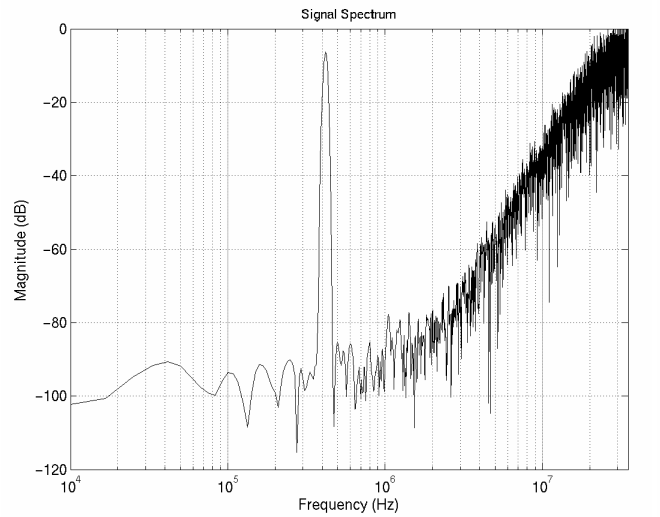


Figure 11a. Output spectra for Bluetooth.

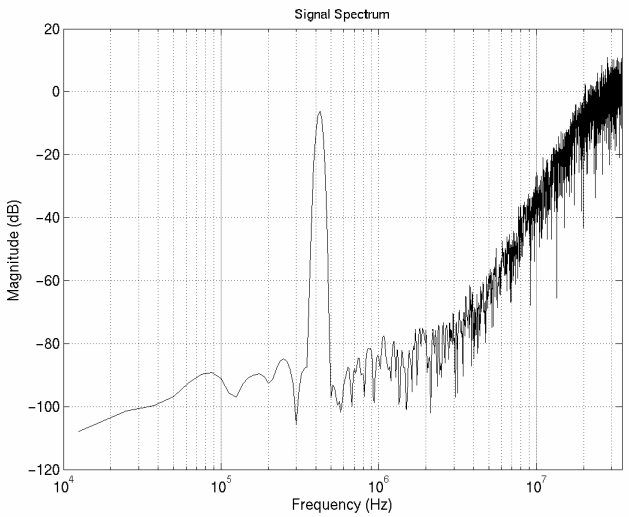


Figure 11b. Output spectra for WCDMA.

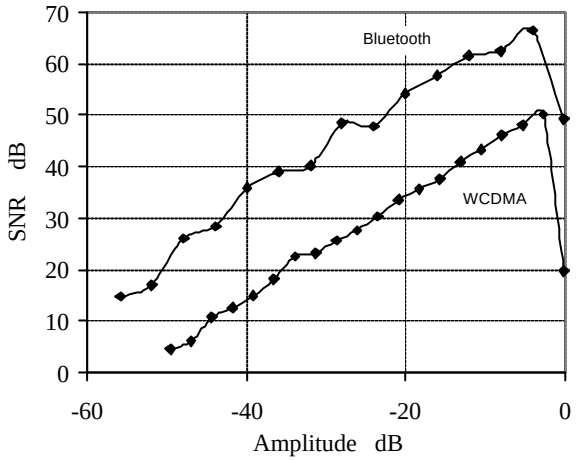


Figure 12. *SNR* vs. relative input amplitude.

We expect that these performance figures be confirmed experimentally and, consequently, the presented design will be located within of the state of the art of SI ΣΔ modulator. This is illustrated in figure 13, where the Figure-of-Merit (FOM)

$$FOM = \frac{Pow}{2^B (2F_{BW})} \tag{8}$$

was used to quantify the quality of the modulators, where *Pow* is the power consumption, *B* is the effective resolution (bits) and F_{BW} is the signal bandwidth. Note that the presented design achieve the higher signal bandwidth reported to now for SI ΣΔ modulators.

CONCLUSIONS

This paper presented the design and electrical implementation of a 1.8-V, 0.18µm CMOS reconfigurable SI ΣΔ modulator for multistandard (Bluetooth/WCDMA) applications. Reconfiguration strategies are used at both architecture level and circuit level in order to minimize the power consumption for each operation mode. Time-domain transistor level simulation results are shown, featuring 11 bit dynamic range within 1MHz and 7.8bit dynamic range within 3.8MHz. If these results are confirmed by experimental measurements, the presented circuit will be competitive with the current state of the art of SI ΣΔ modulators

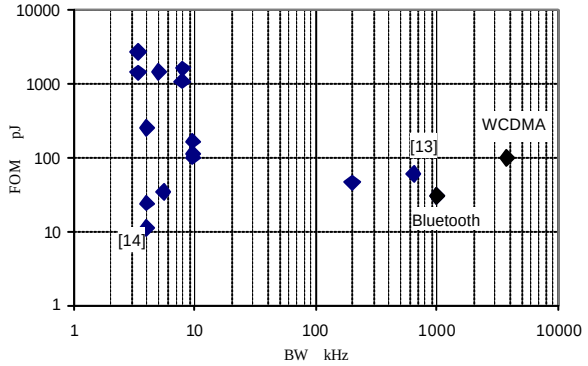


Figure 13. State of the art in SI ADCs.

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