Reliable Analysis of Settling Errors in SC Integrators – Application to High-Speed Low-Power ΣΔ Modulators Design

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Abstract

This paper presents a detailed study on the transient response of SC integrators taking into account the effects of amplifier finite gain-bandwidth product and slew-rate during, unlike previous models, both the integration and sampling phases. Results are applied to the design of high-speed low-power ΣΔ modulators and simplified equations are obtained for manual-estimation of the settling error power.

1. Introduction

As sampling frequency in ΣΔModulators (ΣΔMs) increases in order to cope with XDSL specifications – demanding high-resolution high-speed low-power operation – integrator defective settling becomes one of the most limiting factors in present SC designs. In this scenario, knowing and quantifying the main mechanisms degrading the settling of SC integrators is therefore mandatory.

Although most SC integrator models [1]-[5] take into account the amplifier finite gain-bandwidth product (*GB*) and slew-rate (*SR*), they do so only for the integration phase, while errors derived from the sampling dynamic are omitted, leading to an under-estimation of defective settling specially important in high-speed applications. The SC integrator model considered in [6] includes all former errors, but the developed study is centered on filter design and cannot be easily extended to the case of ΣΔMs.

This paper focuses on the analysis of the transient response of a general SC integrator model during both the integration and sampling phases, giving also compact expressions for a precise estimation of settling errors limiting the performance of high-speed ΣΔMs.

2. Transient Response of SC Integrators

2.1. SC Integrator Model

In order to make a reliable analysis of the transient response of SC integrators, the generic scheme considered, illustrated in Fig.1, includes:

- *i* input branches connected to switching input voltage levels, V_{i1} and V_{i2},
- the parasitic capacitor C_p associated to the summation node,
- the capacitive load C_l associated to the amplifier output node and to the bottom plate of the integration capacitor C_o, as well as,
- *j* branches of an assumed integrator connected to its output during the sampling phase, which has switched to input levels V_{nj2} during the previous integration phase.

On the other hand, the amplifier, depicted in Fig.2, is considered to have:

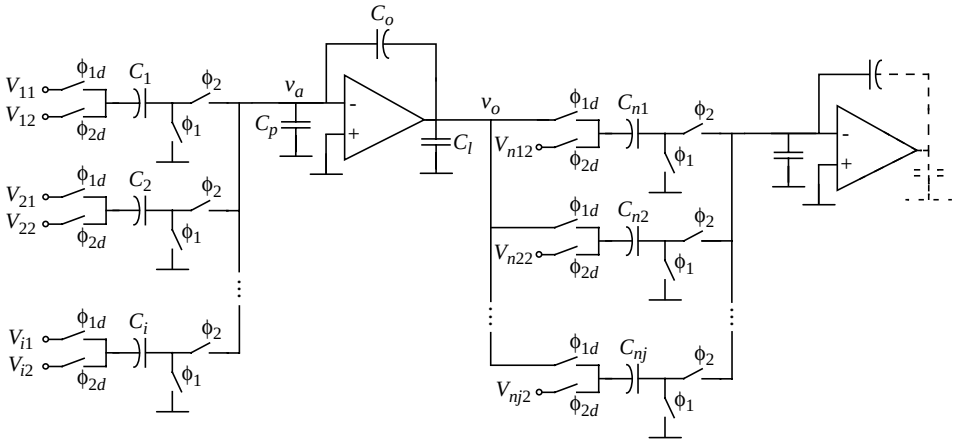

Fig. 1: SC integrator model.

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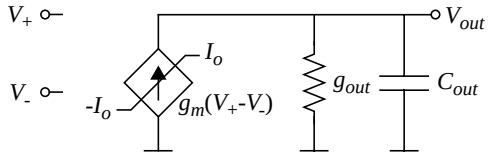

Fig. 2: Amplifier model.

- a non-linear static characteristic, providing a maximum output current I_o, and
- a single-pole dynamic.

With this model for the SC integrator, the amplifier *GB* and *SR* limitations are taken into account, as well as parasitic capacitors associated to its input and output nodes. Moreover, capacitive load at the integrator output is considered to change from the integration to the sampling phase, what reflects the actual situation in most SC sections.

2.2. Integration Phase

Considering respectively $v_{a,\,n-1}$ and $v_{o,\,n-1}$ as the amplifier input and output voltages at the end of the preceding sampling phase, at the beginning of the integration phase, $t = 0$, charge-conservation imposes a jump on these voltages to values

$$\begin{aligned} v_{ai,\,i} &= \frac{\left(1+\frac{C_l}{C_o}\right)}{C_{eq,\,i}}[(V_{12}-V_{11})C_1+\ldots \\ &\quad \ldots+(V_{i2}-V_{i1})C_i]+\frac{C'}{C_{eq,\,i}}v_{a,\,n-1} \\ v_{oi,\,i} &= v_{o,\,n-1}+\frac{C_o}{C_o+C_l}(v_{ai,\,i}-v_{a,\,n-1}) \end{aligned} \tag{1}$$

with $C' = C_p + C_l\left(1+\frac{C_p}{C_o}\right)$ and $C_{eq,\,i}$ referring to the equivalent capacitive load at the amplifier output during the integration phase, given by

$$\begin{aligned} C_{eq,\,i} &= C_p + C_1 + \ldots + C_i + \\ &\quad + C_l\left(1+\frac{C_p+C_1+\ldots+C_i}{C_o}\right) \end{aligned} \tag{2}$$

Note from eq.(1) that v_a and v_o jump at the beginning of this phase in the opposite direction to their final values (see Fig.3). It must be also remarked that, unlike previous models [1]-[5], we have considered $v_{a,\,n-1} \neq 0$, which reflects the possibility of having this node incompletely discharged by the end of the preceding sampling phase.

Depending on the value of the initial amplifier input voltage two possibilities can be distinguished:

(a) $|v_{ai,\,i}| \le \frac{I_o}{g_m}$, where I_o stands for the amplifier maximum output current and g_m for its transconductance. The amplifier will then operate linearly and its input node discharges exponentially following

$$v_a(t) = v_{ai,\,i}\exp\left(-\frac{g_m}{C_{eq,\,i}}t\right) \tag{3}$$

where $g_m \gg g_{out}$ has been supposed.

(b) $|v_{ai,\,i}| > \frac{I_o}{g_m}$, so that the amplifier slews and its input node will then evolve linearly following:

$$v_a(t) = v_{ai,\,i} - \frac{I_o}{C_{eq,\,i}}\,\mathrm{sgn}(v_{ai,\,i})\,t \tag{4}$$

The slewing will go on until $t = t_{o,\,i}$, when the condition for the amplifier to start operating linearly, $v_a(t_{o,\,i}) = I_o/g_m$, fulfills. From this condition we get

$$t_{o,\,i} = \frac{C_{eq,\,i}}{I_o}|v_{ai,\,i}| - \frac{C_{eq,\,i}}{g_m} \tag{5}$$

and from then on $v_a(t)$ will relax exponentially:

$$v_a(t) = \frac{I_o}{g_m}\,\mathrm{sgn}(v_{ai,\,i})\exp\left[-\frac{g_m}{C_{eq,\,i}}(t-t_{o,\,i})\right] \tag{6}$$

During the integration phase $v_o(t)$ is given by

$$\begin{aligned} v_o(t) &= v_{o,\,n-1} - \left(1+\frac{C_p}{C_o}\right)v_{a,\,n-1} - \\ &\quad - \frac{C_1}{C_o}(V_{12}-V_{11}) - \ldots - \frac{C_i}{C_o}(V_{i2}-V_{i1}) + \\ &\quad + \left(1+\frac{C_p+C_1+\ldots+C_i}{C_o}\right)v_a(t) \end{aligned} \tag{7}$$

where $v_a(t)$ stands for eq.(3), (6) or (4) depending, respectively, on the amplifier linear operation, partial- or complete-slewing in this phase.

At the end of the integration phase, $t = T_s/2$, v_a and v_o will be given by eq.(8).

2.3. Sampling Phase

Taking $v_a(T_s/2)$ and $v_o(T_s/2)$, respectively, as the amplifier input and output voltages at the end of the preceding integration phase, at $t = T_s/2$ charge-conservation imposes† a new jump on these voltages to

$$\begin{aligned} v_{ai,\,s} &= v_a\left(\frac{T_s}{2}\right) - \frac{C_{n1}}{C_{eq,\,s}}\left[v_o\left(\frac{T_s}{2}\right) - V_{n12}\right] - \ldots \\ &\quad \ldots - \frac{C_{nj}}{C_{eq,\,s}}\left[v_o\left(\frac{T_s}{2}\right) - V_{nj2}\right] \\ v_{oi,\,s} &= v_o\left(\frac{T_s}{2}\right) + \left(1+\frac{C_p}{C_o}\right)\left[v_{ai,\,s} - v_a\left(\frac{T_s}{2}\right)\right] \end{aligned} \tag{9}$$

†. For simplicity purposes, next integrator input node has been supposed totally relaxed by the end of the preceding integration phase.

$$v_a\left(\frac{T_s}{2}\right) = \begin{cases} v_{ai,\,i}\exp\left(-\dfrac{g_m}{C_{eq,\,i}}\dfrac{T_s}{2}\right) & , |v_{ai,\,i}| \le \dfrac{I_o}{g_m} \\ v_{ai,\,i} - \dfrac{I_o}{C_{eq,\,i}}\mathrm{sgn}(v_{ai,\,i})\dfrac{T_s}{2} & , \dfrac{T_s}{2} \le t_{o,\,i} \\ \dfrac{I_o}{g_m}\mathrm{sgn}(v_{ai,\,i})\exp\left[-\dfrac{g_m}{C_{eq,\,i}}\left(\dfrac{T_s}{2} - t_{o,\,i}\right)\right] & , \dfrac{T_s}{2} > t_{o,\,i} \end{cases} \quad , |v_{ai,\,i}| > \frac{I_o}{g_m} \tag{8}$$

$$v_o\left(\frac{T_s}{2}\right) = v_{o,\,n-1} - \left(1 + \frac{C_p}{C_o}\right)v_{a,\,n-1} - \frac{C_1}{C_o}(V_{12} - V_{11}) - \ldots - \frac{C_i}{C_o}(V_{i2} - V_{i1}) + \left(1 + \frac{C_p + C_1 + \ldots + C_i}{C_o}\right)v_a\left(\frac{T_s}{2}\right)$$

where $C_{eq,\,s}$ refers to the equivalent capacitive output load during the sampling phase, given by

$$C_{eq,\,s} = C_p + (C_l + C_{n1} + \ldots + C_{nj})\left(1 + \frac{C_p}{C_o}\right) \tag{10}$$

Note from eq.(9) that v_a and v_o again jump in the opposite direction to their final values (see Fig.3).

Depending on the initial amplifier input voltage, two more possibilities can be distinguished:

(a) $|v_{ai,\,s}| \le \dfrac{I_o}{g_m}$, and the amplifier operates linearly:

$$v_a(t) = v_{ai,\,s}\exp\left[-\frac{g_m}{C_{eq,\,s}}\left(t - \frac{T_s}{2}\right)\right] \tag{11}$$

(b) $|v_{ai,\,i}| > \dfrac{I_o}{g_m}$, so that the amplifier slews and its input node will then evolve linearly following:

$$v_a(t) = v_{ai,\,s} - \frac{I_o}{C_{eq,\,s}}\mathrm{sgn}(v_{ai,\,s})\left(t - \frac{T_s}{2}\right) \tag{12}$$

The slewing will go on until $t = t_{o,\,s}$, when $v_a(t_{o,\,s}) = I_o/g_m$ fulfills and the amplifier starts operating linearly. From this condition we get

$$t_{o,\,s} = \frac{T_s}{2} + \frac{C_{eq,\,s}}{I_o}|v_{ai,\,s}| - \frac{C_{eq,\,s}}{g_m} \tag{13}$$

and from then on $v_a(t)$ will relax exponentially:

$$v_a(t) = \frac{I_o}{g_m}\mathrm{sgn}(v_{ai,\,s})\exp\left[-\frac{g_m}{C_{eq,\,s}}(t - t_{o,\,s})\right] \tag{14}$$

During the sampling phase $v_o(t)$ is given by

$$v_o(t) = v_o\left(\frac{T_s}{2}\right) + \left(1 + \frac{C_p}{C_o}\right)\left[v_a(t) - v_a\left(\frac{T_s}{2}\right)\right] \tag{15}$$

where $v_a(t)$ stands for eq.(11), (14) or (12) depending, respectively, on the amplifier linear operation, partial- or complete-slewing during this phase.

At the end of the sampling phase, $t = T_s$, v_a and v_o will be given by eq.(16).

2.4. Overall Integration-Sampling Process

The former study on the SC integrator dynamics in the integration and the sampling phases can be easily concatenated, so that the transient evolution of the integrator output voltage is accurately described for the overall integration-sampling process. Nine different evolutions can be obtained for the complete process, which are summarized in Table 1. The actual response the SC integrator follows, out of the nine possible‡, will mainly depend on the input signals level as well as on the amplifier static characteristics.

Ideally, v_o at the end of the process would be,

$$v_{o,n} = v_{o,n-1} - \frac{C_1}{C_o}(V_{12} - V_{11}) - \ldots - \frac{C_i}{C_o}(V_{i2} - V_{i1}) \tag{17}$$

while the actual $v_{o,\,n}$ can be obtained for each possible evolution by the linking of its equations during the sampling phase to those of the preceding integration

‡. Although possible, evolutions 3 and 7 are unlikely to occur in practice, since they imply a huge change on the values of capacitors in the connected SC sections.

$$v_a(T_s) = \begin{cases} v_{ai,\,s}\exp\left(-\dfrac{g_m}{C_{eq,\,s}}\dfrac{T_s}{2}\right) & , |v_{ai,\,s}| \le \dfrac{I_o}{g_m} \\ v_{ai,\,s} - \dfrac{I_o}{C_{eq,\,s}}\mathrm{sgn}(v_{ai,\,s})\dfrac{T_s}{2} & , T_s \le t_{o,\,s} \\ \dfrac{I_o}{g_m}\mathrm{sgn}(v_{ai,\,s})\exp\left[-\dfrac{g_m}{C_{eq,\,s}}(T_s - t_{o,\,s})\right] & , T_s > t_{o,\,s} \end{cases} \quad , |v_{ai,\,s}| > \frac{I_o}{g_m} \tag{16}$$

$$v_o(T_s) = v_o\left(\frac{T_s}{2}\right) + \left(1 + \frac{C_p}{C_o}\right)\left[v_a(T_s) - v_a\left(\frac{T_s}{2}\right)\right]$$

TABLE 1: Possible evolutions during the integration-sampling process

	INTEGRATION		SAMPLING	
1	Linear	eq.(3)	Linear	eq.(11)
2	Partial-slew	eq.(6)	Linear	eq.(11)
3	Slew	eq.(4)	Linear	eq.(11)
4	Linear	eq.(3)	Partial-slew	eq.(14)
5	Partial-slew	eq.(6)	Partial-slew	eq.(14)
6	Slew	eq.(4)	Partial-slew	eq.(14)
7	Linear	eq.(3)	Slew	eq.(12)
8	Partial-slew	eq.(6)	Slew	eq.(12)
9	Slew	eq.(4)	Slew	eq.(12)

phase (see Table 1). Every term obtained for the actual $v_{o,n}$, different from those in eq.(17), derives from an incomplete settling, due to the amplifier finite *GB* and *SR*. Fig.3 shows an evolution with a partial-slewing during both clock-phases and illustrates the influence of the sampling dynamics. Considering only the integration phase would lead in this case to an under-estimation of the defective settling error, since the deviation of the settled voltage is higher at the end of the sampling phase than it was at the end of the integration phase. Equations for all nine cases match with HSPICE results with less than 1% error.

3. Application to ΣΔMs Design

3.1. Comparison with Previous Models through Behavioral Simulations

As the conversion rate increases to cope with specifications demanding high-resolution and high-speed operation, defective settling errors due to amplifiers finite *GB* and *SR* become one of the most limiting factors in present ΣΔMs designs. Moreover, these must be achieved with a reduced power consumption, so that the amplifier dynamic features should be kept as less demanding as possible with no degradation on the modulator performance. This has been traditionally accomplished allowing a certain

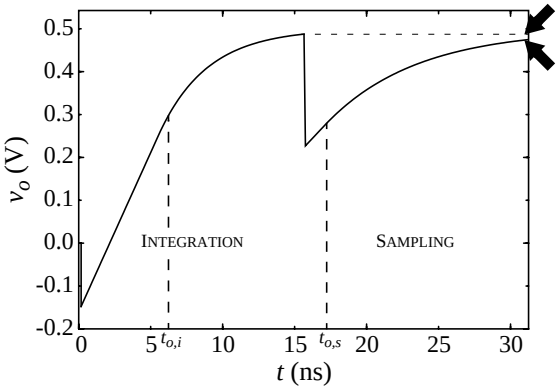

Fig. 3: Transient evolution of integrator output voltage.

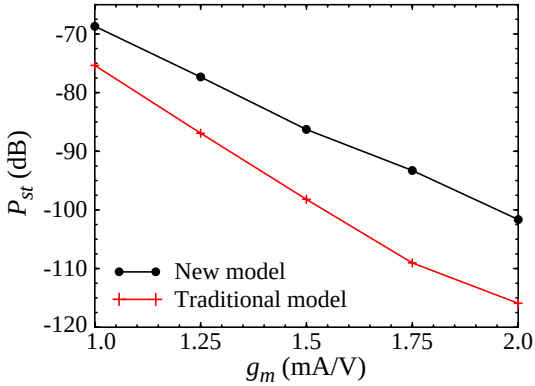

Fig. 4: Comparison of models applied to a 2-1^3*mb* ΣΔM. (V_{in} = 0.5V, I_o = 0.5mA, C_1 = C_p = 0.5pF, C_o = 2pF, C_l = 1pF, C_{ntot} = 1.5pF)

slewing on the amplifier [2][4], what relaxes the amplifier characteristics and does not imply a severe loss of dynamic range in the ΣΔM.

Although amplifiers finite *GB* and *SR* are taken into account in most SC integrator models [1]-[5], this only applies for the integration phase, omitting errors due to the sampling dynamic that become important as the operating frequencies increase.

The new model for the SC integrator and the equations describing its transient response, developed in Section 2, have been introduced in ASIDES [4], a behavioral simulation tool for SC ΣΔMs. Simulations have been carried out on a 12bit@4MSamples/s 2-1^3*mb* cascade ΣΔM [7], operating with sampling frequency f_s = 32MHz, oversampling ratio M = 8, last-stage quantizer resolution B = 4 and reference levels $\pm V_r = \pm 1V$. Fig.4 shows a comparison of the in-band error power due to defective settling, P_{st}, for both traditional and new models as a function of the amplifier transconductance. Note that not considering errors induced during the sampling phase gives too optimistic results, leading in this case to an under-estimation on P_{st} of around 12dB.

3.2. Manual Estimations of Settling Error Power

Integrators defective settling has generally been modeled in ΣΔMs as an error source at the integrator input, so that only the first integrator in the modulator is considered in an approximated analysis. This can be done since the contribution of the rest of integrators to the in-band error power is attenuated by increasing powers of the oversampling ratio [4]. Fig.5 shows the deviation of the settled output voltage at the first integrator in the 2-1^3*mb* ΣΔM from its ideal value, eq.(17). This deviation approximates to a gaussian distribution when the input signal amplitude A approaches the reference voltage V_r. Taking into account this and the equations formerly developed for the transient response of SC integrators, we will try to translate them into compact expressions for the settling error power in SC ΣΔMs.

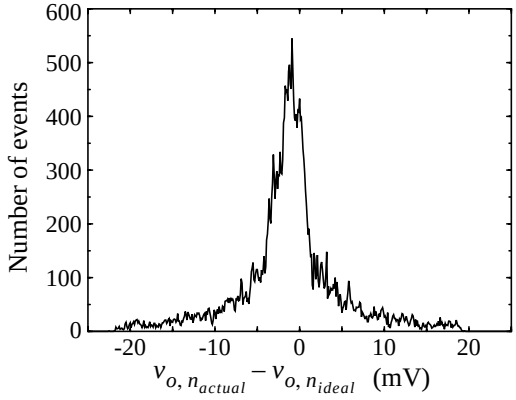

Fig. 5: Histogram of the error in settled voltage. (A = 0.75V, V_r = 1V)

The voltage that the integrator output settles to has been re-written in the following way,

$$v_{o,n} = v_{o,n-1}(1+\varepsilon_o) + \frac{C_{itot}}{C_o} v_{in}(1+\varepsilon_g) + \varepsilon_{off} \quad (18)$$

mapping deviations into:

- a hold-error on the initial output voltage, ε_o,
- a gain-error, ε_g, and
- an offset-error, ε_{off},

with $\frac{C_{itot}}{C_o} v_{in} = -\frac{C_1}{C_o}(V_{12} - V_{11}) - \ldots - \frac{C_i}{C_o}(V_{i2} - V_{i1})$.

Although the obtaining of compact expressions has been done for all nine possible evolutions in the integration-sampling process, we will only consider the first case as an illustrative example.

If the amplifier operates linearly during both clock-phases (case 1 in Table 1), the value of the former errors turns out to be,

$$\begin{aligned}
\varepsilon_o &= -\left(1+\frac{C_p}{C_o}\right)\frac{C_{ntot}}{C_{eq,s}}\exp\left(-\frac{T_s}{2\tau_s}\right) \\
\varepsilon_g &= -\frac{C_{itot}}{C_{eq,i}}\left(1+\frac{C_l}{C_o}\right)\exp\left(-\frac{T_s}{2\tau_i}\right) - \\
&\quad -\left(1+\frac{C_p}{C_o}\right)\frac{C_{ntot}}{C_{eq,s}}\exp\left(-\frac{T_s}{2\tau_s}\right)
\end{aligned} \quad (19)$$

$$\varepsilon_{off} = \left(1+\frac{C_p}{C_o}\right)\frac{C_{n1}V_{n12} + \ldots + C_{n2j}V_{nj2}}{C_{eq,s}}\exp\left(-\frac{T_s}{2\tau_s}\right)$$

where $\tau_i = C_{eq,i}/g_m$, $\tau_s = C_{eq,s}/g_m$, $C_{itot} = C_1 + \ldots + C_i$, $C_{ntot} = C_{n1} + \ldots + C_{nj}$ and terms in $\left[\exp\left(-\frac{T_s}{2\tau_i}\right)\right]\cdot\left[\exp\left(-\frac{T_s}{2\tau_s}\right)\right]$ and in $v_{a,n-1}$ have been neglected.

The actual implementation of the first two integrators in the 2-1^3*mb* ΣΔM is shown in Fig.6. When compared to the SC integrator model considered in Fig.1, we get that $V_{11} = v_{in}$, $V_{12} = V_{n22} = \pm V_r$ and $V_{n12} = 0$. In this situation, worst case will then occur for $v_{in} > 0$ when $V_{12} = V_{n22} = -V_r$ ††, so that

$$\begin{aligned}
\varepsilon_o &= -\left(1+\frac{C_p}{C_o}\right)\frac{C_{ntot}}{C_{eq,s}}\exp\left(-\frac{T_s}{2\tau_s}\right) \\
\varepsilon_g &= -\frac{C_1}{C_{eq,i}}\left(1+\frac{C_l}{C_o}\right)\exp\left(-\frac{T_s}{2\tau_i}\right) - \\
&\quad -\left(1+\frac{C_p}{C_o}\right)\frac{C_{ntot}}{C_{eq,s}}\exp\left(-\frac{T_s}{2\tau_s}\right) \\
\varepsilon_{off} &= -\left(1+\frac{C_p}{C_o}\right)\frac{C_{n2}}{C_{eq,s}}V_r\exp\left(-\frac{T_s}{2\tau_s}\right)
\end{aligned} \quad (20)$$

- On the one hand, ε_g and ε_{off} can be considered as error sources that add to the modulator input signal and, therefore, are not attenuated in the baseband. Considering, as in [5], that these errors correspond to three times their standard deviation in a gaussian distribution, and that they are uniform in the range ($-f_s/2$, $f_s/2$), we get:

$$\begin{aligned}
\sigma_g &= \frac{\varepsilon_g}{3} v_{in} \quad \Rightarrow \quad S_g(f) = \frac{\sigma_g^2}{f_s} = \frac{\varepsilon_g^2}{9 f_s} v_{in}^2 \\
\sigma_{off} &= \frac{\varepsilon_{off}}{3} \quad \Rightarrow \quad S_{off}(f) = \frac{\sigma_{off}^2}{f_s} = \frac{\varepsilon_{off}^2}{9 f_s}
\end{aligned} \quad (21)$$

Integrating in the baseband, we get their contributions to the defective settling error power,

††. Results will be analogous if $V_{12} = V_{n22} = V_r$ for $v_{in} < 0$.

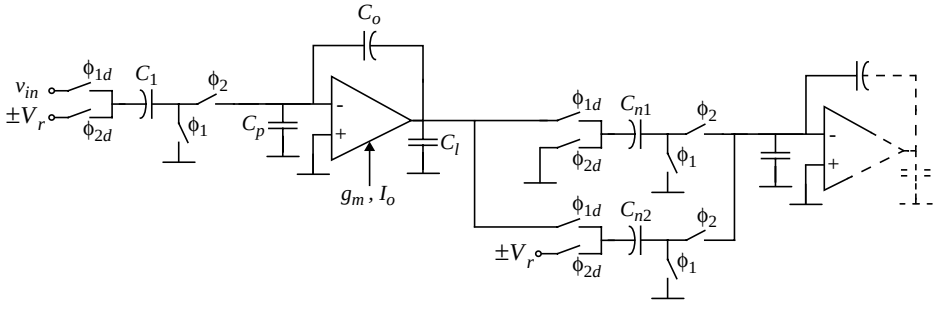

Fig. 6: Implementation of first and second integrators in the 2-1^3*mb* ΣΔM.

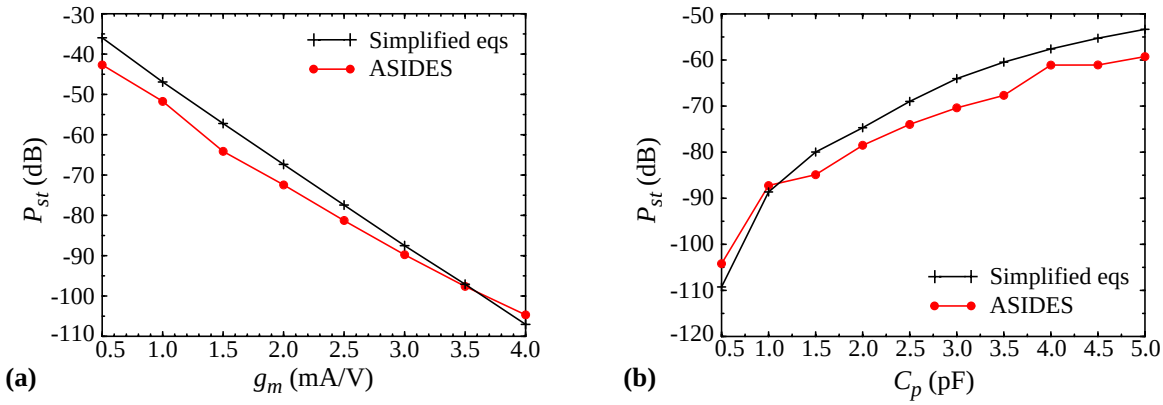

Fig. 7: Comparison of simplified equations and behavioral simulation results for the 2-1^3*mb* ΣΔM:
(a) Variation of g_m (V_{in} = 0.5V, I_o = 0.75mA, C_1 = 0.5pF, C_o = 2pF, C_l = 1pF, C_p = 1.5pF, C_{ntot} = 2pF)
(b) Variation of C_p (V_{in} = 0.6V, g_m = 2mA/V, I_o = 0.25mA, C_1 = 0.5pF, C_o = 2pF, C_l = 1pF, C_{ntot} = 1pF)

$$P_g = \frac{A^2}{9M}\left[\frac{C_1}{C_{eq,\,i}}\left(1+\frac{C_l}{C_o}\right)\exp\left(-\frac{T_s}{2\tau_i}\right)+ + \left(1+\frac{C_p}{C_o}\right)\frac{C_{ntot}}{C_{eq,\,s}}\exp\left(-\frac{T_s}{2\tau_s}\right)\right]^2 \quad (22)$$

$$P_{off} = \frac{V_r^2}{9M}\left(1+\frac{C_p}{C_o}\right)^2\left(\frac{C_{n2}}{C_{eq,\,s}}\right)^2\exp\left(-\frac{T_s}{\tau_s}\right)$$

where A is the input signal amplitude.

- On the other hand, error ε_o translates into a memory error that will basically affect the noise transfer function of the modulator. Considering only this error term, the integrator output at the end of the integration-sampling process will be,

$$v_{o,\,n} = v_{o,\,n-1}(1+\varepsilon_o) + g_1 v_{in,\,n-1} \quad (23)$$

where $g_1 = C_1/C_o$.

The integrator transfer function will then be,

$$\frac{v_o(z)}{v_{in}(z)} = \frac{g_1 z^{-1}}{1-z^{-1}(1+\varepsilon_o)} \quad (24)$$

so that the following expression, valid for cascade ΣΔMs [4], can be derived for its contribution to P_{st},

$$P_o = \frac{\Delta_1^2}{12}\cdot\frac{\pi^{2L_1-2}L_1}{(2L_1-1)M^{2L_1-1}}\left(\frac{\varepsilon_o}{3}\right)^2 \quad (25)$$

where Δ_1 is the quantization step of the comparator in the first-stage of the cascade and L_1 is the first-stage order. For the 2-1^3*mb* ΣΔM, this leads to:

$$P_o = \frac{2V_r^2}{27}\cdot\frac{\pi^2}{3M^3}\cdot\left(1+\frac{C_p}{C_o}\right)^2\left(\frac{C_{ntot}}{C_{eq,\,s}}\right)^2\exp\left(-\frac{T_s}{\tau_s}\right) \quad (26)$$

The total in-band error power due to defective settling will then finally be given by:

$$P_{st} = P_o + P_g + P_{off} \quad (27)$$

A comparison between simplified equations and results obtained by behavioral simulation in ASIDES is carried out in Fig.7 for a wide range of variation on the amplifier transconductance and its input parasitic. Note the high agreement of the obtained P_{st}. Moreover, simplified equations present the additional advantage of being a bit conservative when compared to more accurate behavioral simulation results, what may be very practical for a hand-made estimation of the required integrator dynamics.

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