# A CMOS 110-dB@40-kS/s Programmable-Gain Chopper-Stabilized Third-Order 2-1 Cascade Sigma-Delta Modulator for Low-Power High-Linearity Automotive Sensor ASICs

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***Abstract*—This paper describes a 0.35-$\mu$m CMOS chopper-stabilized switched-capacitor 2-1 cascade $\Sigma\Delta$ modulator for automotive sensor interfaces. The modulator architecture has been selected from an exhaustive comparison among multiple topologies in terms of resolution, speed and power dissipation. To obtain a better fitting with the characteristics of different sensor outputs, the circuit can be digitally programmed to yield four input-to-output gain values ($\times 0.5, \times 1, \times 2$, and $\times 4$) and has been designed to operate within the stringent environmental conditions of automotive electronics (temperature range of $-40\,^{\circ}$C to $175\,^{\circ}$C). In order to relax the amplifier's dynamic requirements for the different modulator input-to-output gains, switchable capacitor arrays are used for all the capacitors in the first integrator. The design of the building blocks is based on a top-down CAD methodology which combines simulation and statistical optimization at different levels of the modulator hierarchy. The circuit is clocked at 5.12 MHz and the overall power consumption is 14.7 mW from a single 3.3-V supply and occupies 5.7 mm$^2$ silicon area. Experimental results show a maximum SNR of 87.3 dB within a 20-kHz signal bandwidth and 90.7 dB for 10-kHz signals, and an overall DR of 110 and 113.8 dB, respectively. These performance features place the reported circuit at the cutting edge of state-of-the-art high-resolution $\Sigma\Delta$ modulators.**

***Index Terms*—Analog-to-digital conversion, sigma-delta modulation, mixed analog-digital integrated circuits, sampled data circuits.**

## I. Introduction

During the last few years there has been a significant increase in the use of electronic sensory systems for the automotive [1]. This is partially fuelled by advances in MEMS technology and the possibility to combine sensors together with DSPs on the same package and even the same chip [2]. Linked to this trend, the necessity arises to design CMOS analog front-ends (AFEs), and specifically analog-to-digital converters (ADCs), capable of coping with the stringent requirements of the automotive industry.

Fig. 1 shows a typical conceptual block diagram for an automotive sensor chip. On the one hand, the converter must be compliant with a very large temperature range, typically ([$-40\,^{\circ}$C, $175\,^{\circ}$C]), and with many other hostile environmental issues [3]–[5]. On the other hand, the AFE must cope with weak signals (ranging from microvolts to hundreds of milivolts) in the presence of large temperature and process dependent offset. The changing amplitude range of the input signal can be handled through programmable gain—similar to what happens in multipurpose sensors [5]. Also, large accuracy and bandwidths up to 10–20 kHz are needed at the ADC to increase the quality of the information delivered to the DSP, and hence the smartness of the system [2].

It is advised that $\Sigma\Delta$-based ADCs are used to handle these challenges due to different reasons:

- They are better suited than full Nyquist ADCs to achieve high resolution (16–17 bit) in the band of interest with moderate power consumption [6], [7].
- The action of feedback renders sigma-delta modulators ($\Sigma\Delta$Ms) very linear, and high linearity is a must for automotive applications.
- The behavior of some sensing devices fits well to $\Sigma\Delta$-based ADCs, thus easing partial or total integration of the sensor within the converter [8], [9].
- $\Sigma\Delta$Ms can incorporate programmable gain without significant degradation.

However, detailed modeling of circuit nonidealities and involved design plans are needed to take advantage of all these potentials while addressing the stringent environmental and robustness requirements. Actually, several $\Sigma\Delta$Ms that digitize 20–25 kHz signals with medium-to-high resolution have been reported [10]–[13]. To the best of our knowledge, the highest resolution (18.7 bits) is featured by the modulator in [11], whereas the lowest power consumption is reported in [12], which targets 14 bits within a 20-kHz signal bandwidth. In all these cases, the modulator input-to-output gain[1] was fixed to unity.

This paper reports a programmable-gain chopper-stabilized third-order cascade (2-1) $\Sigma\Delta$M in a 3.3-V 0.35-$\mu$m CMOS technology. Its design relies upon detailed behavioral modeling and the use of an advanced top-down methodology that combines multilevel behavioral simulation and statistical optimization at different levels of the hierarchy [7]. Experimental results show correct operation in a 20-kHz bandwidth ($B_w$)

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[1]In the following, the term "modulator input-to-output gain" will be referred to as "modulator gain".

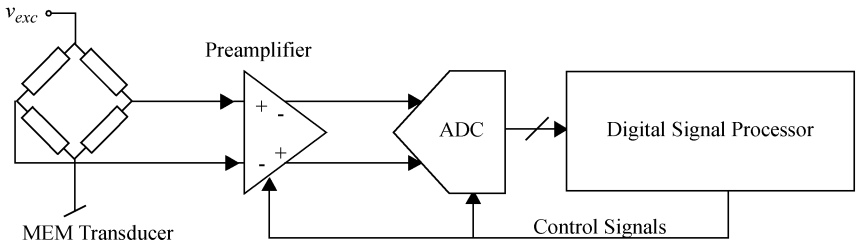



Fig. 1. Conceptual block diagram of a "smart" sensor chip.

with 110-dB overall dynamic range (DR), and 113.8-dB DR within $B_w = 10$ kHz. These figures locate this circuit at the cutting edge of state-of-the-art CMOS $\Sigma\Delta$Ms. Also, the herein reported modulator IC is one of the few high-resolution circuits with embedded programmable gain reported to date.

This paper is organized as follows. Section II describes general design considerations. Section III applies those considerations to the proper selection of the modulator architecture and obtains a set of optimized specs for the constituent building blocks. These specs are inputs for the electrical design of the circuit cells, which are covered in Section IV. Finally, Section V gives experimental results and compares the performance of the chip with current state-of-the-art designs.

## II. Basic Design Considerations

We choose expandible cascade architectures to implement the modulator [14]. These architectures are advisable as they do not raise stability issues and permit an input voltage amplitude that is close to the theoretical full-scale (FS) input range of the modulator without causing overloading. Actually, the family of expandible cascades exhibits a signal-to-noise ratio (SNR) peak at $-5$ dBFS regardless of the actual modulator order [14].[2] This helps to handle the changing dynamic range of the sensor signals. Besides, cascade architectures can incorporate a multibit quantizer without resorting to dynamic element matching (DEM) or any other linearization technique [7]. Furthermore, they can be designed by following quite modular, prone- to-optimization plans [14]. Finally, cascade architectures constitute a mature technology demonstrated for a variety of industrial cutting-edge designs [5], [10], [16], [17].

The in-band error power of whatever cascade $\Sigma\Delta$M can be expressed as [7]

$$P_{\text{in-band}} \cong P_Q + P_{\text{cn}} + P_{\text{nl}} + P_{\text{st}} \tag{1}$$

where $P_Q$ stands for the quantization error, $P_{\text{cn}}$ for the circuit noise error, $P_{\text{nl}}$ for the nonlinearity error, and $P_{\text{st}}$ for the defective settling error. $\Sigma\Delta$Ms can be designed such that the quantization error dominates, i.e., such that the following condition is fulfilled:

$$P_{\text{cn}} + P_{\text{nl}} + P_{\text{st}} \ll P_Q \cong \frac{1}{12}\left[\frac{2V_{\text{ref}}}{(2^B-1)}\right]^2 \frac{\pi^{(2L)}}{(2L+1)\cdot M^{(2L+1)}} \tag{2}$$

[2]The use of multibit quantization in every stage of the cascade modulator might result in SNR peaks close to the theoretical FS voltage [15]. However, linearization techniques need to be used in order to reduce the nonlinearity of the internal D/A converters.

where the right term shows the quantization error, neglecting leakage, as a function of the modulator order $(L)$, the oversampling ratio $(M)$, and the number of bits in the internal quantizer $(B)$. $V_{\text{ref}}$ stands for the FS reference voltage of the $\Sigma\Delta$M.

In our case, and given the high accuracy target, to make the quantization error dominate would lead to huge power consumption and area occupation. Instead, it is more efficient to make the design such that $P_Q \cong P_{\text{cn}} + P_{\text{nl}} + P_{\text{st}}$. Two basic considerations arise related to this criterion: first, to make a comparative balance among the several circuit error contributions; second, to find expression linking the dominant circuit errors to the circuit design parameters. Regarding the balance and owing to the limited bandwidth it can be assumed that $P_{\text{st}} \ll P_{\text{cn}}$. Besides, since the available supply voltage grants large enough room for signal excursion, it can be assumed that $P_{\text{nl}} \ll P_{\text{cn}}$. Under these assumptions, the basic design criterion reduces itself to equalize the quantization error and the circuit noise error, i.e., $P_Q \cong P_{\text{cn}}$.

Let us now focus on the expression of the circuit noise error as a function of the circuit design parameters. Consider to that purpose the conceptual schematic of the two-branch switched-capacitor (SC) integrator in Fig. 2, where the input branch and the DAC feedback branch employ different capacitors respectively to implement a modulator gain $\xi = C_{s1}/C_{s2}$. The main contributors to the noise error are the operational transconductance amplifier (OTA) thermal and flicker noise, and the switch on-resistance thermal noise. Also, noise coming from the $V_{\text{ref}}$ generation block must be accounted for as a combination of white noise and flicker noise [18].

Flicker noise will be handled at the architectural level by applying chopper techniques [4], [5], so that only white noise remains to dictate electrical design considerations; i.e., $P_{\text{cn}} \approx P_{\text{wn}}$. Careful analysis including folding mechanisms shows that the input white noise power spectral density (PSD) at the input of each branch of the fully differential circuitry can be approximated at low frequencies by [19]

$$\begin{aligned} S_{\text{in},C_{s1}}(f) &\cong \frac{4kT}{C_{s1}f_S} + \frac{4kT(1+n_t)}{3C_{\text{eq},i}f_S} \\ S_{\text{in},C_{s2}}(f) &\cong \frac{4kT}{C_{s2}f_S} + \frac{4kT(1+n_t)}{3C_{\text{eq},i}f_S} + \frac{kT}{C_{s2}f_S}\cdot\frac{R_{\text{eq,ref}}}{2R_{\text{on}}} \end{aligned} \tag{3}$$

where $k$ is the Boltzman constant, $T$ is the absolute temperature, and $R_{\text{on}}$ is the switch on-resistance. The first term in each equation above contains the contribution of all the switches in the

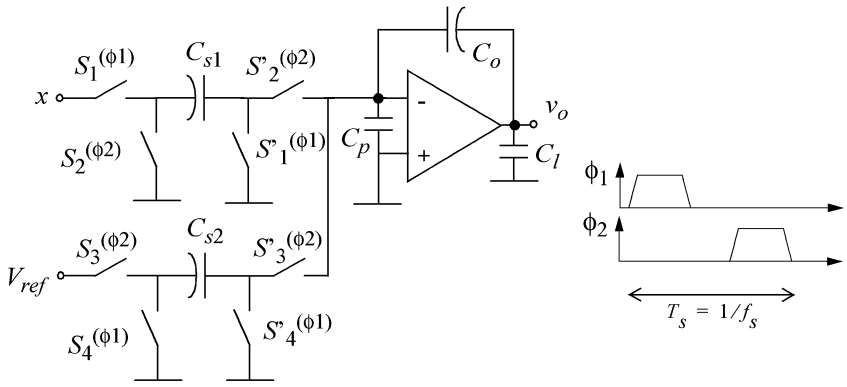



Fig. 2. Two-branch SC integrator.

corresponding branch. The second term accounts for the OTA contribution, where

$$C_{\mathrm{eq},i} = C_p + C_{s2}(1+\xi) + C_l\left[1 + \frac{C_p + C_{s2}(1+\xi)}{C_o}\right] \quad (4)$$

is the OTA equivalent load during the integration phase, while $\phi_2$ is high. When estimating the white noise PSD of the OTA, the contributions of MOS devices other than the input ones are compiled in the factor $n_t$, which equals the summation of the respective transconductance ratios. The third term in the expression of $S_{\mathrm{in},C_{s2}}$ represents the noise coming from $V_{\mathrm{ref}}$, where $R_{\mathrm{eq,ref}}$ is its equivalent noise resistance.

By neglecting contributions other than those of the first integrator in the cascade, the $\Sigma\Delta$M output white noise power is obtained as

$$P_{\mathrm{wn}} \cong \frac{4kT}{MC_{s2}}(1+\xi) + \frac{4kT(1+n_t)}{3MC_{\mathrm{eq},i}}(1+\xi)^2 + \frac{kT}{MC_{s2}}\frac{R_{\mathrm{eq,ref}}}{2R_{\mathrm{on}}}. \quad (5)$$

Quantitative analysis of (5) shows that the white noise power increases with the $\Sigma\Delta$M gain, $\xi$. In practice, this means that as the gain increases, the capacitances must be increased as well, and thus does the power consumption. This is worsened because as $\xi$ increases, the OTA equivalent load increases [see (4)] and hence, more power is needed to meet the dynamic requirements.

Seeking minimum power consumption dictates setting $\xi$ as close as possible to unity. Actually, for $\xi = 1$, the two branches in Fig. 2 can be merged into one, thus further reducing $P_{\mathrm{wn}}$ and, consequently, $C_{\mathrm{eq},i}$. This is the choice commonly found in literature [5]. However, such a choice implies that in a sensor A/D interface like that shown in Fig. 1, the programmability must be incorporated into the preamplifier, rendering its design more complicated.

In the application under consideration, the automotive sensor interface must accommodate a huge range of signal amplitudes (130 dB below full scale) within a 20-kHz bandwidth. For this purpose, the preamplifier is designed with a fixed gain of $\times 10$, whereas the $\Sigma\Delta$ modulator can be digitally programmed to yield four gain values—$\times 0.5, \times 1, \times 2$, and $\times 4$. This solution simplifies the architecture and design of the preamplifier, which in this case consists of a resistor-feedback instrumentation topology—*a priori* a less demanding design than using a programmable-gain ($\times 5, \times 10, \times 20$, and $\times 40$) amplifier based on switchable elements (capacitors or resistors), given the stringent noise and linearity requirements.

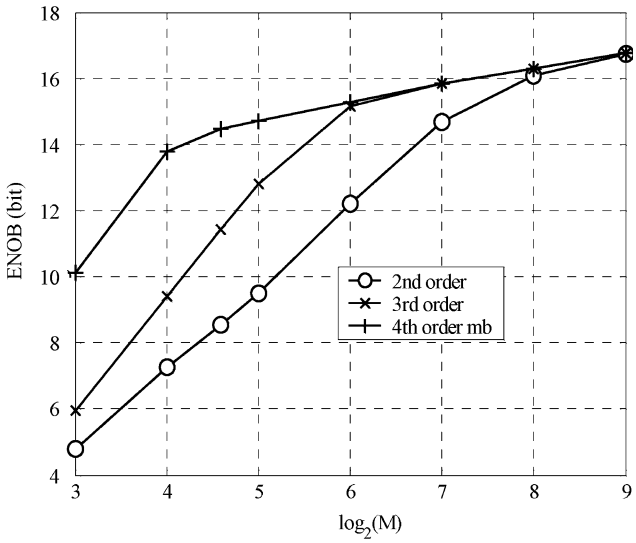



Fig. 3. Effective number of bits (ENOB) versus oversampling ratio for three $\Sigma\Delta$ Ms: fourth-order 3-bit ($L = 4, B = 3$), third-order 1-bit ($L = 3, B = 1$) and second-order 1-bit ($L = 2, B = 1$).

## III. Architecture Selection and High-Level Sizing

Architecture selection involves three parameters, namely oversampling ratio $(M)$, loop order $(L)$, and the resolution of the internal quantizer $(B)$. These three parameters univocally define an instance of the general expandible $2 - 1^{L-2}$ cascade architecture [14].[3]

How are the values of these parameters chosen? A first observation is that, for every value of $L$ and $B$, as $M$ increases there is a transition from one region where $P_Q \gg P_{\mathrm{wn}}$ into another where $P_Q \ll P_{\mathrm{wn}}$. It is illustrated in Fig. 3, which shows the effective resolution of three $\Sigma\Delta$Ms as a function of $M$. The same front-end integrator is used for the three cases. For each curve there is a breakpoint where $P_Q \cong P_{\mathrm{wn}}$. Above this breakpoint, within the region dominated by white noise, doubling $M$ generates a mere 3 dB decrease in the in-band error power. Below this breakpoint the decrease of the error with $M$ depends on the

[3]The term $2 - 1^{L-2}$ is used in this paper to denote a $L$th-order cascade modulator formed by a second-order stage followed by $L-2$ identical first-order stages.

TABLE I
OUTCOME OF THE ΣΔM ARCHITECTURE SELECTION PROCEDURE

| ΣΔM Gain, $\xi$ | Order ($L$)[a] | Oversampling Ratio ($M$) | Estimated Power Consumption (mW) |
|---|---|---|---|
| 0.5 | 3 | 128 | 6.77 |
| | 3 | 256 | 8.12 |
| | 4 | 128 | 8.27 |
| 1 | 3 | 128 | 8.48 |
| | 3 | 256 | 9.77 |
| | 4 | 128 | 10.32 |
| 2 | 3 | 128 | 12.69 |
| | 3 | 256 | 13.85 |
| | 2 | 512 | 13.88 |
| 4 | 2 | 512 | 23.24 |
| | 3 | 128 | 24.21 |
| | 3 | 256 | 25.02 |

a. All ΣΔMs in this table are cascade 2-1$^{L-2}$ architectures except for $L = 2$.

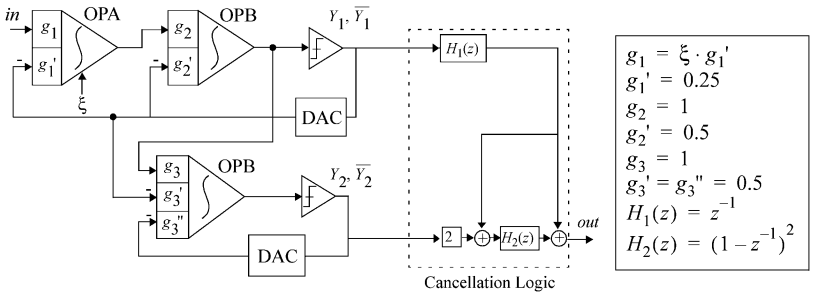



Fig. 4. Block diagram of the programmable-gain 2–1 cascade SC ΣΔM.

actual values of $L$ and $B$. The only way to shift the breakpoint up is by enlarging the sampling capacitor.

This observation provides rationale supporting the choice of $P_Q \cong P_{\rm wn}$, namely:

- within the region dominated by quantization noise, the sampling capacitor, and hence the demands on building block dynamics, area and power, are larger than needed;
- within the region dominated by white noise, oversampling becomes less inefficient (only a fraction $1/M$ of the noise power falls into the signal bandwidth) and either $L$ or $B$, or both, may allow a reduction without significant impact on resolution.

Actually, most state-of-the-art circuits are designed to operate close to but at the right side of this breakpoint [7].

A second qualitative observation is related to the choice of $M$. On the one hand, the condition $P_Q \cong P_{\rm wn}$ defines an univocal relationship between each $\{L, B\}$ pair and $M$. On the other hand, since the targeted bandwidth is medium to low, constraints on $M$ are not strong. This means that there are fairly large degrees of freedom to set $M, L$, and $B$. As a rule of thumb, since the targeted resolution is only moderately high, the oversampling ratio does not need to be extremely high. This means that the breakpoint in Fig. 3 can be moved to the left, providing room for many possible combinations of $B$ and $L$.

Actual architecture selection is driven by power minimization, based on the following iterative procedure:

1) For given values of $L, M, B, V_{\rm ref}$, and $\xi$, calculate $P_Q$ and select $C_{s2}$ so that $P_Q + P_{\rm wn}$ is smaller than the maximum allowed in-band error power.
2) Estimate $C_{{\rm eq},i}$ from (4). Then, use a linear settling model with settling constant $C_{{\rm eq},i}/g_m$ to estimate the required OTA transconductance, taking into account that it takes a number $\ln(2^{\rm ENOB})$ of time constants to settle within effective number of bits (ENOB) resolution.
3) Relate the OTA $g_m$ with its power dissipation, for which the candidate OTA topology must be known *a priori*. A suitable selection is closely linked to the process technology: supply voltage, minimal device length, etc. Potential choices are a folded-cascode OTA up to 3-V supply, and a two-stage amplifier below 2.5 V [20].
4) Once the first integrator power dissipation is estimated, that of the remaining integrators (in practice with less demanding specifications) can be estimated as a fraction of it. The overall static power is then obtained by adding up all the contributions.

For realistic estimation, this procedure is fine-tuned by including the impact of other nonideal effects (such as finite and nonlinear OTA DC-gain, slew-rate, errors in the multibit quantizers, etc.), the power dissipated in other blocks, and the dynamic power dissipation [14], [16].

### A. Modulator Architecture

Previous design considerations have been applied for the target specs of 40 kS/s and DR $\geq$ 110 dB. A large number of architectures have been compared in terms of the estimated power consumption and silicon area. The outcome of the comparison, summarized in Table I for ΣΔMs with a 1-bit internal quantizer, led us to choose the third-order 2-1 cascade ΣΔM shown in Fig. 4 with $M \geq 128$. Note from Table I that the

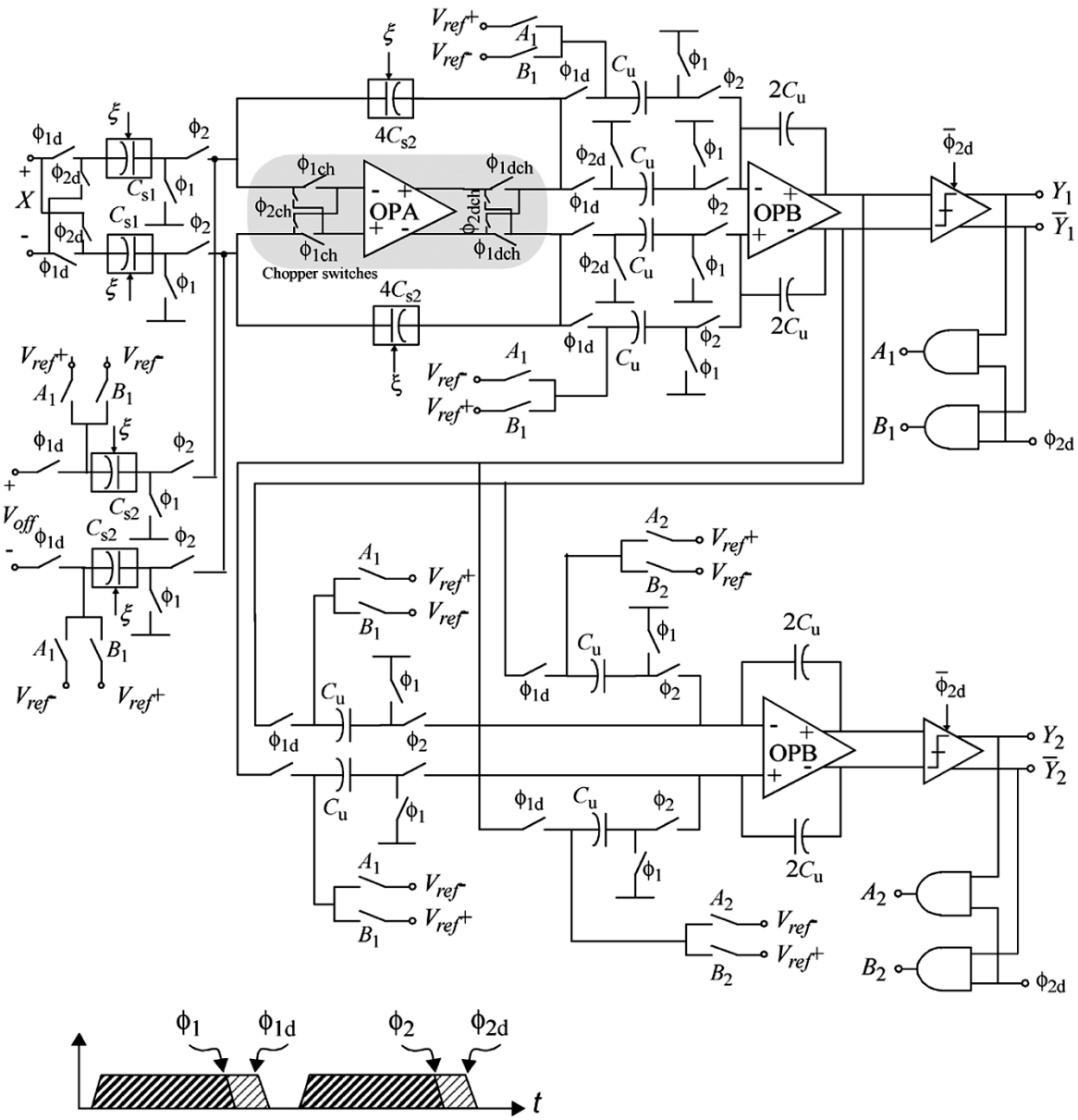



Fig. 5. SC fully differential schematic of the 2–1 cascade SC $\Sigma\Delta$M in this paper.

architecture in Fig. 4 obtains the best results, except for $\xi = 4$. In this case, the lowest power consumption is obtained by a second-order $\Sigma\Delta$M with $M = 512$, the third-order cascade being the second one in the ranking. However, the second-order architecture does not qualify for some values of $\xi$. Also, it requires a four times faster clock than the cascade, thereby increasing the issues related to substrate noise coupling.

### *B. SC Implementation*

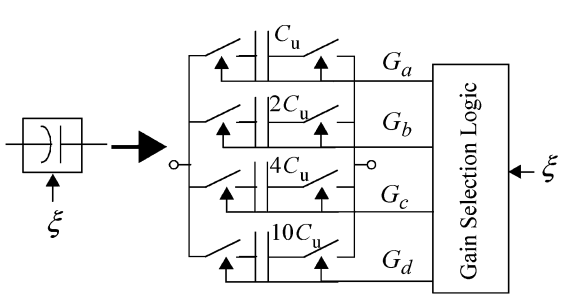
Fig. 5 shows the fully differential SC schematic of the selected $\Sigma\Delta$M architecture. Note that the SC branch connected to the input signal in the first integrator uses double sampling to achieve an extra gain of 2, without increasing circuit noise [21]. The other branch receives the digital-to-analog converter (DAC) outputs. Making use of the spare connection of this branch, an external DC signal ($V_{\rm off}$) can be applied during $\phi_1$ to center the sensor signal in the modulator full-scale range. This solution renders unnecessary a third branch for offset compensation; it can therefore be eliminated, and results in no further increase of thermal noise.

The second stage of the modulator incorporates an integrator with only two input branches, although three different weights are implemented: $g_3, g_3'$, and $g_3''$ (see Fig. 4). This can be done because the selection of weights in the designed modulator, considering that $g_3/g_3' = g_3/g_3''$, allows the distribution of weight $g_3 = 1$ between the two integrator branches, namely $g_3' = 0.5$ and $g_3'' = 0.5$.

The modulator operation is controlled by two nonoverlapped clock phases, namely sampling phase $\phi_1$ and integration phase $\phi_2$. In order to attenuate the signal-dependent clock feedthrough, delayed versions of the two phases ($\phi_{1\rm d}$ and $\phi_{2\rm d}$) are also provided. As illustrated in Fig. 5, this delay is incorporated only to the falling edges of the clock phases (i.e., to the turn-off of the switches), while the rising edges are

| $\xi$ | $C_{s1}$ | $C_{s2}$ | $C_o$ | $G_a$ | $G_b$ | $G_c$ | $G_d$ |
|---|---|---|---|---|---|---|---|
| 0.5 | $C_u$ | $4C_u$ | $16C_u$ | 1 | 0 | 0 | 0 |
| 1 | $2C_u$ | $4C_u$ | $16C_u$ | 0 | 1 | 0 | 0 |
| 2 | $6C_u$ | $6C_u$ | $24C_u$ | 0 | 1 | 1 | 0 |
| 4 | $16C_u$ | $8C_u$ | $32C_u$ | 0 | 1 | 1 | 1 |

**(a)**




**(b)**

Fig. 6. Programmable capacitors in the first integrator. (a) Capacitor arrays. (b) $C_{s1}$ implementation.

synchronized in order to increase the effective time-slot for the modulator operations [17]. The comparators are activated at the end of phase $\phi_2$ (using $\overline{\phi_{2\mathrm{d}}}$ as a strobe signal) to avoid any possible interference due to the transient response of the integrators' outputs at the beginning of the sampling phase. In addition to the master clock phases, $\phi_1$ and $\phi_2$, additional phases are required to control the chopper switches used in the first integrator to attenuate flicker noise. These chopper phases are controlled by a master clock with programmable frequency, as will be described in Section IV.

The programmable gain ($\xi = 0.5, 1, 2$, and 4) has been mapped onto switchable capacitor arrays, each of them formed by a variable number of unitary capacitors ($C_{\mathrm{u}} = 1.5$ pF) as shown in Fig. 6. Such numbers are selected for minimum power dissipation, bearing in mind the circuit noise limitation and the maximum temperature target (175 °C). In order to keep the amplifier dynamic requirements as relaxed as possible, we propose to switch all unitary capacitors instead of just those forming the sampling capacitors. This is based on the following.

- For large gains ($\xi > 1$) $C_{s1}$ is larger than $C_{s2}$. Hence, $P_{\mathrm{wn}}$ is amplified with respect to the unity-gain case as it multiplied by $(1 + C_{s1}/C_{s2})$ [see (5)].
- For low gains ($\xi < 1$) the situation is the contrary. Now $P_{\mathrm{wn}}$ is attenuated with respect to the unity-gain case, which allows us to decrease the capacitance values, mainly $C_{\mathrm{s2}}$. This strategy also relaxes the required amplifier dynamics because its equivalent load capacitance will also be decreased.
- In order to simultaneously handle the modulator gain[4] ($2C_{s1}/C_{s2}$) and the first integrator feedback weight ($C_{s2}/C_o$ always equal to 0.25), the value of all capacitances must be changed by re-arranging the number of unitary capacitors forming them.

### C. High-Level Sizing and Building-Block Specifications

The modulator specifications have been mapped onto building-block specifications using statistical optimization for design parameter selection, and compiled equations (capturing nonideal building-block behavior) for evaluation. This process is fine-tuned by behavioral simulation using an updated version of ASIDES, an advanced behavioral simulator of SC $\Sigma\Delta$Ms [22]. At this step, nonidealities are covered more accurately than when compiled equations are used. Also, worst cases for speed (the largest capacitor values) and for thermal noise (the highest temperature and the lowest capacitor values) are contemplated.

The outcome of this sizing process is summarized in Table II, where OPA denotes the opamp used at the first integrator and OPB refers to the opamps used at the second- and third-integrator (see Fig. 5). The data in Table II show the specifications of the building blocks that define the starting point for the block sizing that will be described in Section IV.

The system-level performance of the modulator has been verified considering the parameters in Table II. Fig. 7 shows the in-band output spectra for the different modulator gains, clocked at $f_S = 5.12$ MHz and considering a $-20$-dBV, 5-kHz input sinewave. The in-band error[5] power is also depicted. The figure shows that the total in-band error is, despite the gain, larger than 100 dB below FS ($V_{\mathrm{ref}} = 2$ V), as required for the proposed application. The DR is boosted by the modulator gain, leading to an overall DR referred to FS (DRFS) larger than 118 dB.

## IV. Design of the Building Blocks

### A. Amplifiers

The key features for the design of the amplifiers are their open-loop DC gain, dynamic requirements and output swing. Regarding the latter, the set of integrator weights used for the $\Sigma\Delta$M in Fig. 5 allow us to relax the output swing requirements to being only slightly larger than the voltage reference (2 V in this case), which is feasible when operating with 3.3-V supply in differential mode.

Table II shows that OPA is more demanding than OPB, the reason being that the contribution of the latter to the total in-band error power is attenuated by the gain of the front-end integrator in the signal band. Thus, to reduce power consumption, OPA and OPB are handled as different instances during the design purposes. For this goal, an improved version of the transistor-level sizing tool FRIDGE [22] was used to explore the potentials of a wide catalog of fully differential OTA topologies. A single-stage folded-cascode architecture, shown in Fig. 8, was selected as

[4]An extra signal gain of 2 is considered as a consequence of using double sampling in the first integrator.

[5]The in-band error power includes noise and distortion caused by circuit error mechanisms.

TABLE II
HIGH-LEVEL SIZING OF THE PROGRAMMABLE-GAIN 2–1 ΣΔM

| SPECS: 110-dB@40kS/s@2$V_p$ | | | Value | Unit |
|---|---|---|---|---|
| INTEGRATORS | Integration capacitor | Gain 0.5 | 24 | pF |
| | | Gain 1 | 24 | pF |
| | | Gain 2 | 36 | pF |
| | | Gain 4 | 48 | pF |
| | Unitary capacitor | | 1.5 | pF |
| | Sigma | | 0.1 | % |
| | Capacitor non-linearity | | 25 | ppm/$V^2$ |
| | Bottom parasitic capacitor | | 5 | % |
| | Switch ON-resistance | | <650 | Ω |
| OPAMPS | DC-gain | OPA | 68 | dB |
| | | OPB | 63 | dB |
| | DC-gain non-linearity | | 15% | $V^{-2}$ |
| | GBW | OPA (44.2pF load) | 17 | MHz |
| | | OPB (8.9pF load) | 15 | MHz |
| | Slew-rate | OPA (44.2pF load) | 17 | V/μs |
| | | OPB (8.9pF load) | 28 | V/μs |
| | Output swing | | ±2.5 | V |
| COMPARATORS | (Hysteresis + Offset) (max.) | | 30 | mV |
| | Resolution time | | 50 | ns |

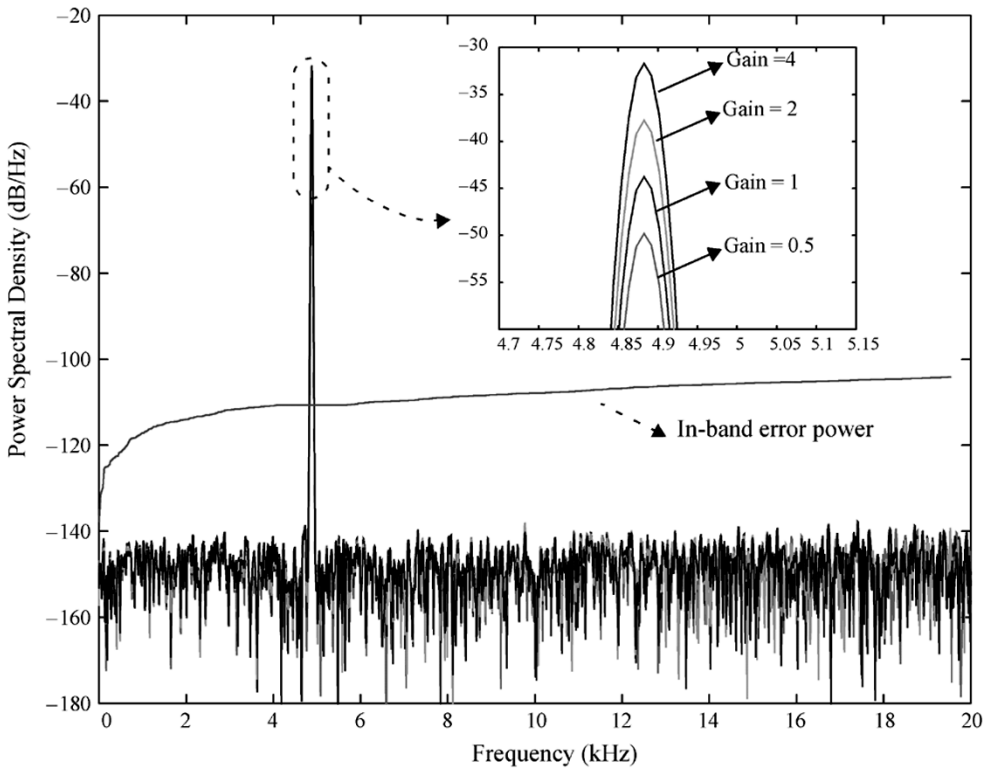



Fig. 7. In-band (20 kHz) simulated output spectra of the proposed ΣΔM (see Fig. 5) for different modulator gains.

a convenient choice for both amplifiers. $N$-channel input transistors were employed to take advantage of the twin-well technology feature in removing the body effect of nMOS transistors. The common-mode feedback (CMFB) net has been implemented using a SC circuit, which provides fast linear operation with small power dissipation.

Table III shows the full sizing and biasing of OPA and OPB. Table IV summarizes the obtained electrical performance for both amplifiers using HSPICE, regarding the target values imposed during the optimization procedure with FRIDGE. The table depicts the parameter values corresponding to typical operation conditions (typical process parameters, nominal supply

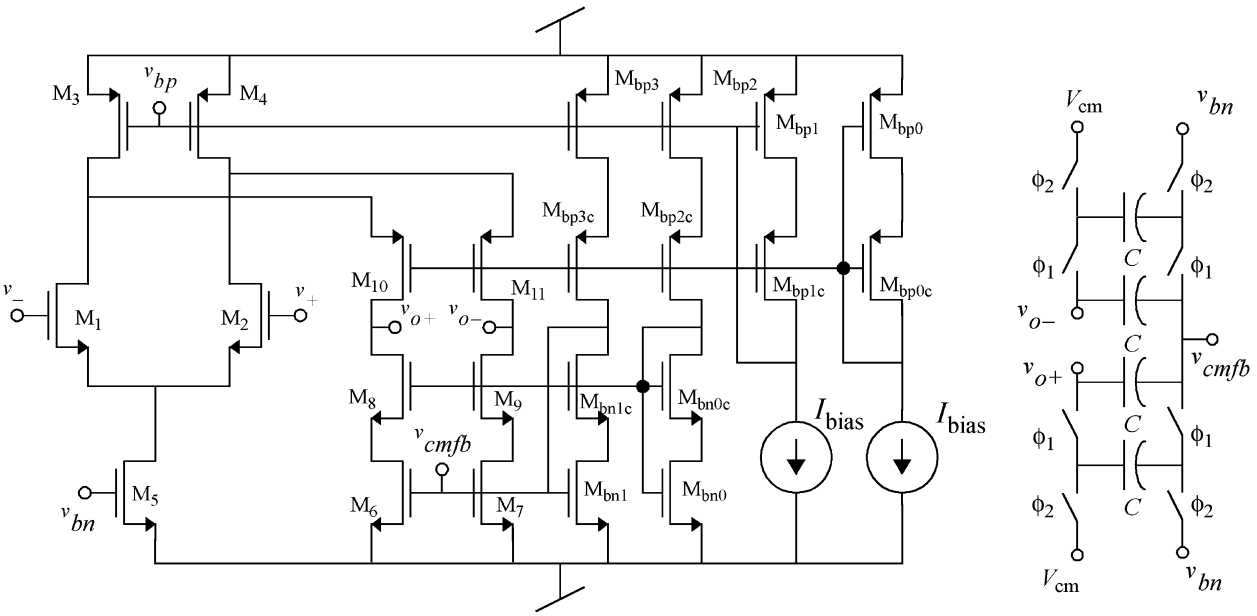



Fig. 8. Fully differential folded-cascode amplifier used in the $\Sigma\Delta$ modulator.

TABLE III
SIZING AND BIASING OF THE OPAMPS

| SIZES | | |
|---|---|---|
| Transistor | OPA (μm/μm) | OPB (μm/μm) |
| $M_{1,2}$ | 5x(40/0.5) | 2x(25/0.5) |
| $M_{3,4}$ | 8x(65.6/0.5) | 8x(25.5/0.5) |
| $M_5$ | 8x(42.5/0.5) | 8x(10.7/0.5) |
| $M_{6,7}$ | 5x(32/0.5) | 5x(8/05) |
| $M_{8,9}$ | 8x(31.05/0.6) | 8x(5.65/0.45) |
| $M_{10,11}$ | 8x(64/0.5) | 8x(30.20/0.45) |
| $M_{bp0}$ | 8.85/0.5 | 4/0.5 |
| $M_{bp1,2,3}$ | 65.6/0.5 | 25.5/0.5 |
| $M_{bpc0,1,2,3}$ | 64/0.5 | 30.20/0.45 |
| $M_{bn0}$ | 4.45/0.5 | 1.9/0.5 |
| $M_{bn1}$ | 42.5/0.5 | 10.7/0.5 |
| $M_{bnc1,2}$ | 31.05/0.6 | 5.65/0.45 |
| BIASING | | |
| $I_{bias}$ (μA) | 110 | 36.7 |

TABLE IV
ELECTRICAL PERFORMANCE OF THE OPAMPS (HSPICE)

| | OPA (45pF load) | | OPB (9pF load) | |
|---|---|---|---|---|
| Model | Typical | Worst-Case | Typical | Worst-Case |
| DC gain (dB) | 74.0 | 71.09 | 68.3 | 68.3 |
| GB (MHz) | 22.6 | 15.8 | 34.4 | 23.8 |
| Phase Margin (°) | 86.4 | 85.5 | 83.5 | 81.4 |
| Slew-Rate (V/μs) | 22.1 | 21.1 | 38.1 | 35.7 |
| Output Swing (V) | ±2.75 | ±2.50 | ±2.75 | ±2.50 |
| Transconductance (mA/V) | 6.30 | 4.50 | 1.95 | 1.35 |
| Power consumption (mW) | 7.1 | 7.2 | 2.3 | 2.4 |

voltage, and room temperature) as well as the worst case value for each parameter in a corner analysis—considering fast and slow device models, ±10% variation in the 3.3-V supply, and temperatures in the range [−40 °C, +175 °C].

The amplifier nonlinear features (mainly nonlinear DC gain and dynamics) deserve special attention in a high-linear implementation. When the amplifier output swings, the drain-to-source voltage of the output transistors changes, and so does the output impedance. This effect, illustrated in Fig. 9 for the OPA and OPB in the nominal conditions, induces a dependence of the open-loop DC gain on the output voltage; the DC gain reaches its maximum at the central point and decreases as the output approaches the rails. Such a nonlinearity is traditionally modeled by second-order polynomial dependence of the gain on the output voltage [7], but this is only valid for small voltage excursions around the central point. On the contrary, in the proposed 3.3-V implementation, it is expected that small-gain regions of the DC curve (around boundaries of shadowed areas in Fig. 9) are often visited during normal operation of the modulator. In order to accurately account for this nonlinearity during behavioral simulations, we have resorted to a table look-up procedure based on amplifier DC curves obtained by electrical simulation. A similar approach has been employed to validate the actual transient response of the front-end integrator.

### B. Comparators

The specifications for the single-bit quantizers (comparators) at the end of the first and second stages of the modulator are given in Table II. In order to cope with the required resolution time (around 50 ns) and hysteresis (lower than 30 mV) a regenerative latch including a pre-amplifying stage was selected [23].

Fig. 10 shows the selected comparator topology. It consists of a nMOS differential input pair $(M_{1-2})$, a CMOS regenerative latch circuit, and a RS flip-flop. The latch circuit is composed of a nMOS flip-flop $(M_{3-4})$ with a pair of nMOS switches $(M_{9-10})$ for strobing and a nMOS switch $(M_{17})$ for resetting, and a pMOS flip-flop $(M_{5-6})$ with a pair of pMOS precharge switches $(M_{7-8})$.

The comparator is activated at the end of the integration phase. At the beginning of the next integration phase, the out-

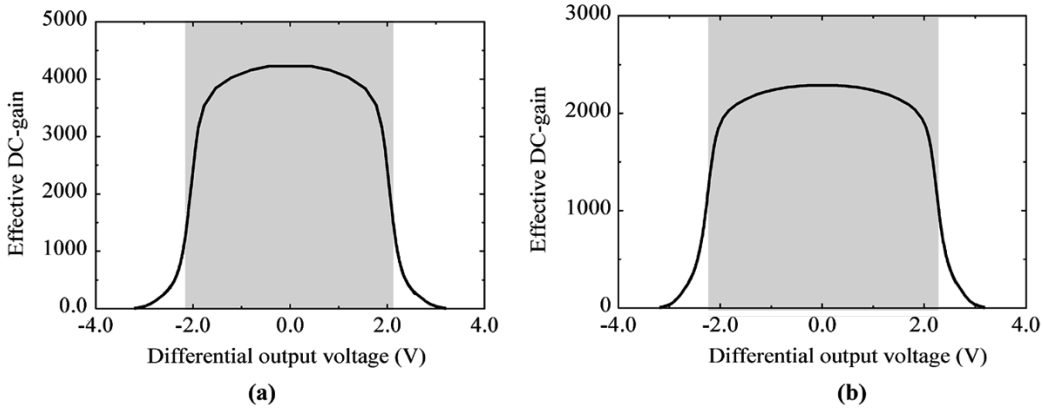



Fig. 9. DC-gain nonlinearity for (a) OPA and (b) OPB.

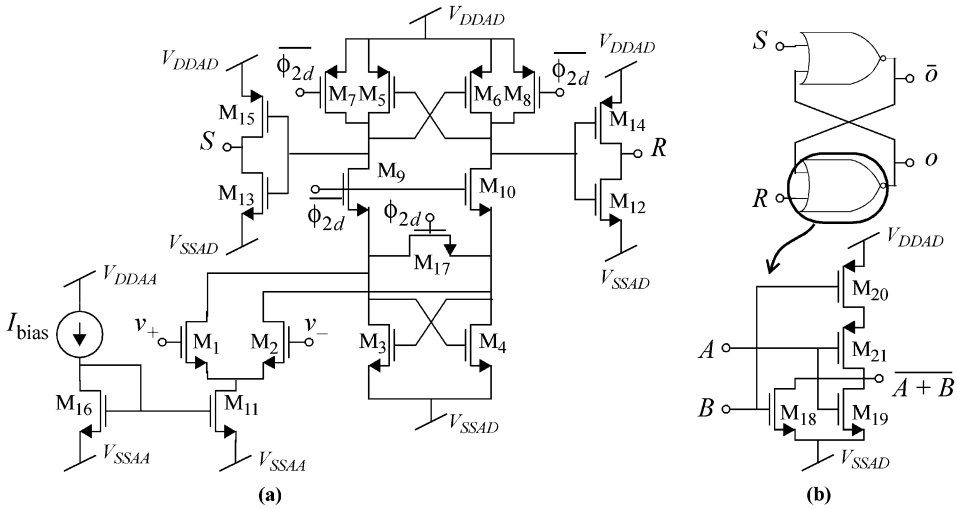



Fig. 10. Schematic of the comparator. (a) Preamplifier + latch. (b) RS flip-flop.

puts of the latch are forced to the low state and the RS flip-flop maintains the comparator output until the next strobbing of the latch. As shown in Fig. 10, different voltage supplies have been used for the pre-amplifier and for the regenerative latch—$V_{\mathrm{DDAA}}$ and $V_{\mathrm{DDAD}}$, respectively. This has been done in order to reduce the comparator sensitivity to injected digital switching noise and supply bounce effects.

The circuit in Fig. 10 has been designed according to the required high-level specifications, while keeping the input capacitance and the power consumption as low as possible. Table V shows the sizes of the transistors and the value of the bias current.

MonteCarlo simulations and corner analysis have been done to extract the comparator performance during sizing. Table VI summarizes its electrical performance, showing the worst cases for hysteresis, offset and resolution time together with the power dissipation. As expected, the resolution is dominated by mismatching, the offset being the dominant limitation factor with a worst case value of 9.92 mV, which is compliant with the specifications in Table II.

TABLE V
SIZING AND BIASING OF THE COMPARATORS

| MOST | W/L (μm/μm) |
|---|---|
| $M_{1,2}$ | 20/0.5 |
| $M_{3,4}$ | 4/2 |
| $M_{5,6}$ | 16/2 |
| $M_{7\text{-}10,12\text{-}15,17}$ | 1.5/0.35 |
| $M_{11,16}$ | 8/1 |
| $M_{18}$ | 6.3/0.35 |
| $M_{19}$ | 4.2/0.35 |
| $M_{20,21}$ | 11.9/0.35 |
| $I_{\mathrm{bias}}$ | 55μA |

### C. Switches

The main design issue related to the switches is the finite switch on-resistance, $R_{\mathrm{on}}$, which is mainly constricted by dynamic considerations. Incomplete settling caused by transmission gates is traditionally reduced by making $R_{\mathrm{on}}C_{s1}f_S \ll 1$. In our circuit, $R_{\mathrm{on}}$ values up to 650 Ω (see Table II) can be tolerated with no degradation of the modulator performance. These values can be obtained using CMOS switches with aspect ratios of $6.5/0.35$ for the nMOS transistor and $23.5/0.35$ for the pMOS, operating with the nominal 3.3-V supply.

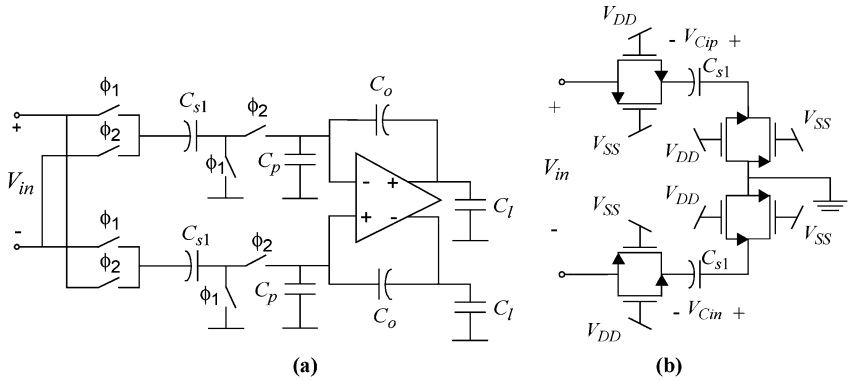



Fig. 11. Analog switches: (a) fully differential SC integrator; (b) circuit under evaluation.

TABLE VI
ELECTRICAL PERFORMANCE OF THE COMPARATORS (HSPICE)

| Parameter | Typical | Worst-case |
|---|---|---|
| Offset (mV) | 0.75 | 9.92 |
| Hysteresis (mV) | 0.03 | 0.12 |
| Resol. time, $T_{RLH}$ (ns) | 4.10 | 8.60 |
| Resol. time, $T_{RHL}$ (ns) | 3.90 | 6.15 |
| Power Consumption (mW) | 0.43 | |

TABLE VII
THD CAUSED BY ANALOG SWITCHES FOR A 1 Vpd AT 20 kHz INPUT TONE

| Model | Temperature (ºC) | THD (dB) |
|---|---|---|
| Slow | -40 | -100 |
| | 25 | -101 |
| | 175 | -102 |
| Typical | -40 | -104 |
| | 25 | -105 |
| | 175 | -107 |
| Fast | -40 | -109 |
| | 25 | -110 |
| | 175 | -112 |

In addition to the $R_{\rm on}$ value, the dependence of this value with voltage must be carefully addressed. This nonlinearity causes dynamic distortion during the sampling process—the larger the sampling capacitor and the signal frequency, the larger the distortion [24]. In our case, the distortion is particularly noticeable for $\xi = 4$, where $C_{s1} = 24$ pF. To keep it under specs, one first possibility is using smaller $R_{\rm on}$ values. However, this leads to prohibitive parasitics and power dissipation. Another possibility is including clock-bootstrapping [25]. However, this increases complexity and leads to a less robust design. Instead, we have studied in depth the sampling process of the first SC integrator [see Fig. 11(a)], seeking optimization. Electrical simulations of the circuit in Fig. 11(b) have been done using corner analysis for a 0 dBV at 20 kHz sine-wave input. The differential voltage stored in capacitors $C_{s1}$ was collected at a rate of 5.12 MHz, and a Kaiser-windowed fast Fourier transform (FFT) was processed.

Table VII summarizes the total harmonic distortion (THD) values obtained during corner analysis. Note that the worst case THD generated by the analog switches is $-100$ dB, which agrees with required specifications. Thus, the sizing used for the CMOS switches in the front-end integrator—with aspect ratios of $29.1/0.35$ for the nMOS transistor and $105.9/0.35$ for the pMOS—ensures a distortion low enough for the present application, and suggests that clock boosting or similar techniques are not required in the technology used.

### D. Capacitor Arrays

Capacitors have been implemented using MIM structures. With this structure, the 1.5-pF unitary capacitor used to implement the integrator weights is approximately 31.6 $\mu$m $\times$ 31.6 $\mu$m in size. The estimated mismatch for this capacitor is $\sigma(\Delta C/C) = 0.1\%$. As mismatch error is one of the most important limiting factors in cascade architectures, common centroid structures have been used in the layout. For the first integrator, all the capacitors ($C_{s1}, C_{s2}$, and $C_0$ in Fig. 6) are made up of unitary capacitors that are connected or disconnected from an array structure depending on the value of the modulator gain. The arrangement of unitary instances in this programmable common-centroid structure is symbolically shown in Fig. 12. On the other hand, the matching of weights $g_2', g_3'$, and $g_3''$ is just based on closely placed unitary capacitors.

### E. Clock-Phase Generators

Two clock-phase generator circuits have been incorporated to the prototype: one of them generates the master clock phases and the other one provides the chopper phases required by the first integrator (see Fig. 5).

Fig. 13 shows the schematics of the two clock-phase generators. Both of them generate two nonoverlapped clock phases $(\phi_1, \phi_2, \phi_{1\rm ch}, \phi_{2\rm ch})$ from an external clock signal CLK. In order to avoid signal-dependent clock feedthrough, delayed versions of the two phases $(\phi_{1\rm d}, \phi_{2\rm d}, \phi_{1\rm dch}, \phi_{2\rm dch})$ are also generated [26]. The complementary versions of these phases are also generated $(\bar{\phi}_{\rm j})$ in order to control the CMOS switches, and all phases are properly buffered at the generators output. A buffer tree is used for that purpose, given the assorted capacitive loads that the different clock phases have to drive. In order to relax the requirements on the integrators' transient response, especially for the case $\xi = 4$, the external clock signal has a duty cycle of 77.5%–22.5% (integration-sampling phases). With the clock

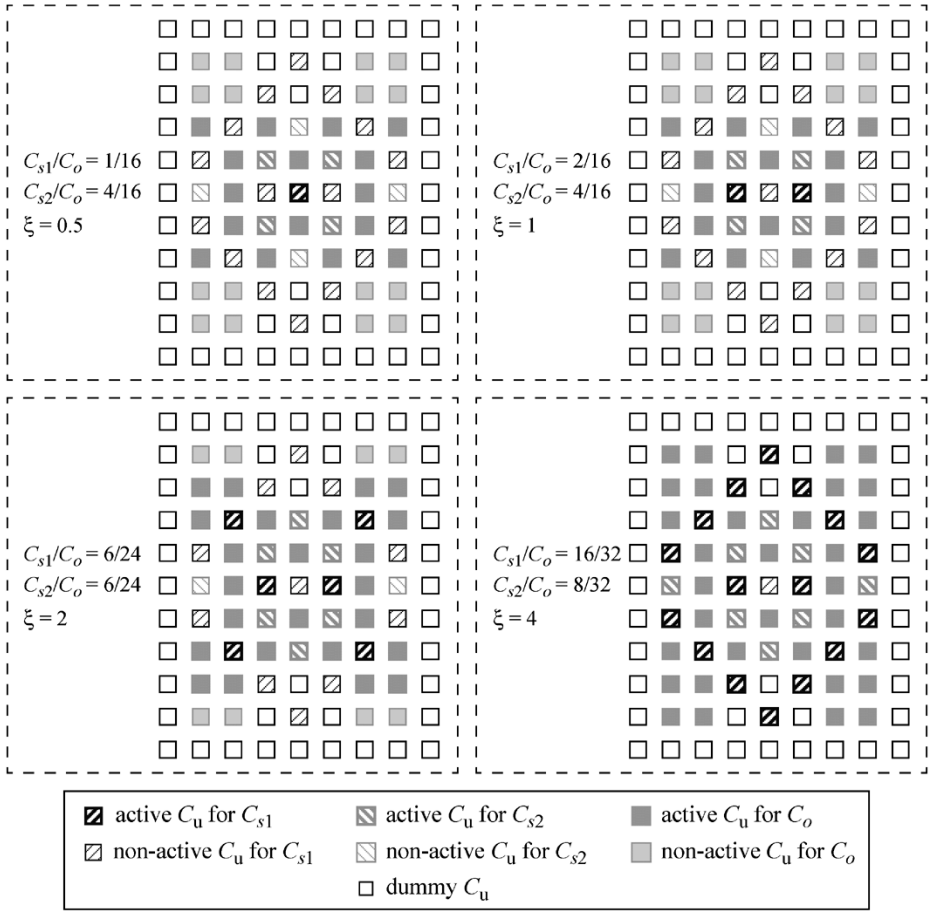



Fig. 12. Conceptual layout of programmable capacitor array of the front-end integrator.

scheme used, conceptually shown in Fig. 13(c), the nonoverlapping time and the delay time are approximately 0.2 ns, while the effective time-slot for integrators operations is 151.37 ns for $\phi_1, \phi_{1d}, \bar{\phi}_1, \bar{\phi}_{1d}$, and 43.54 ns for $\phi_2, \phi_{2d}, \bar{\phi}_2, \bar{\phi}_{2d}$.

## V. Experimental Results

The modulator has been designed and fabricated in a single-poly, five-metal, 0.35-$\mu$m CMOS technology. Fig. 14 shows the complete layout [Fig. 14(a)] and a microphotograph of the main parts of the chip [Fig. 14(b)]. The layout has been carefully designed to maximize the modulator performance according to the following considerations:

- The distance between the most sensitive analog blocks (front-end) and the digital section is the longest possible in order to attenuate the impact of the switching activity.
- Separated analog, mixed, and digital supplies have been used. Analog power supplies have been employed for the current biasing of the analog blocks in the $\Sigma\Delta$ modulator (mainly the amplifiers and the pre-amplifiers stages of the comparators), as well as the voltage biasing of the substrate and wells in the analog section of the chip. Mixed supplies have been dedicated to the integrator switches, the dynamic CMFB nets for the amplifiers and the comparators regenerative latches. Digital power supplies have been used for the biasing of the clock-phase generators and for the two buffers driving the output of the modulator stages out of the chip.
- Guard-rings that surround the analog, mixed, and digital sections of the chip, have been included in order to maintain a low impedance return path and avoid the spreading of digital switching noise to the sensitive parts of the modulator.
- The layout has been kept symmetrical and centroid layout techniques with unitary transistors have been employed for matched transistors in the operational amplifiers, and in the preamplifying stages and regenerative latches of the comparators.

The complete modulator occupies an area of 5.7 mm$^2$ (pads included) and dissipates 14.7 mW from a single 3.3-V supply. The chip is encapsulated in 64-pin plastic quad flat package as illustrated in Fig. 15(a). Double-bonding techniques and multiple pins are used for the power supplies in order to reduce supply bounce.

The circuit has been tested using a printed circuit board (PCB), shown in Fig. 15(b), that includes intensive filtering and decoupling strategies, as well as proper impedance termination to avoid signal reflections. The performance of the modulator was evaluated using a high-resolution ($-$100-dB THD) sinusoidal source to generate the input signal and a digital data acquisition unit to generate the clock signal and to acquire the bit streams of the first and second stages of the $\Sigma\Delta$M. The same unit controlled the

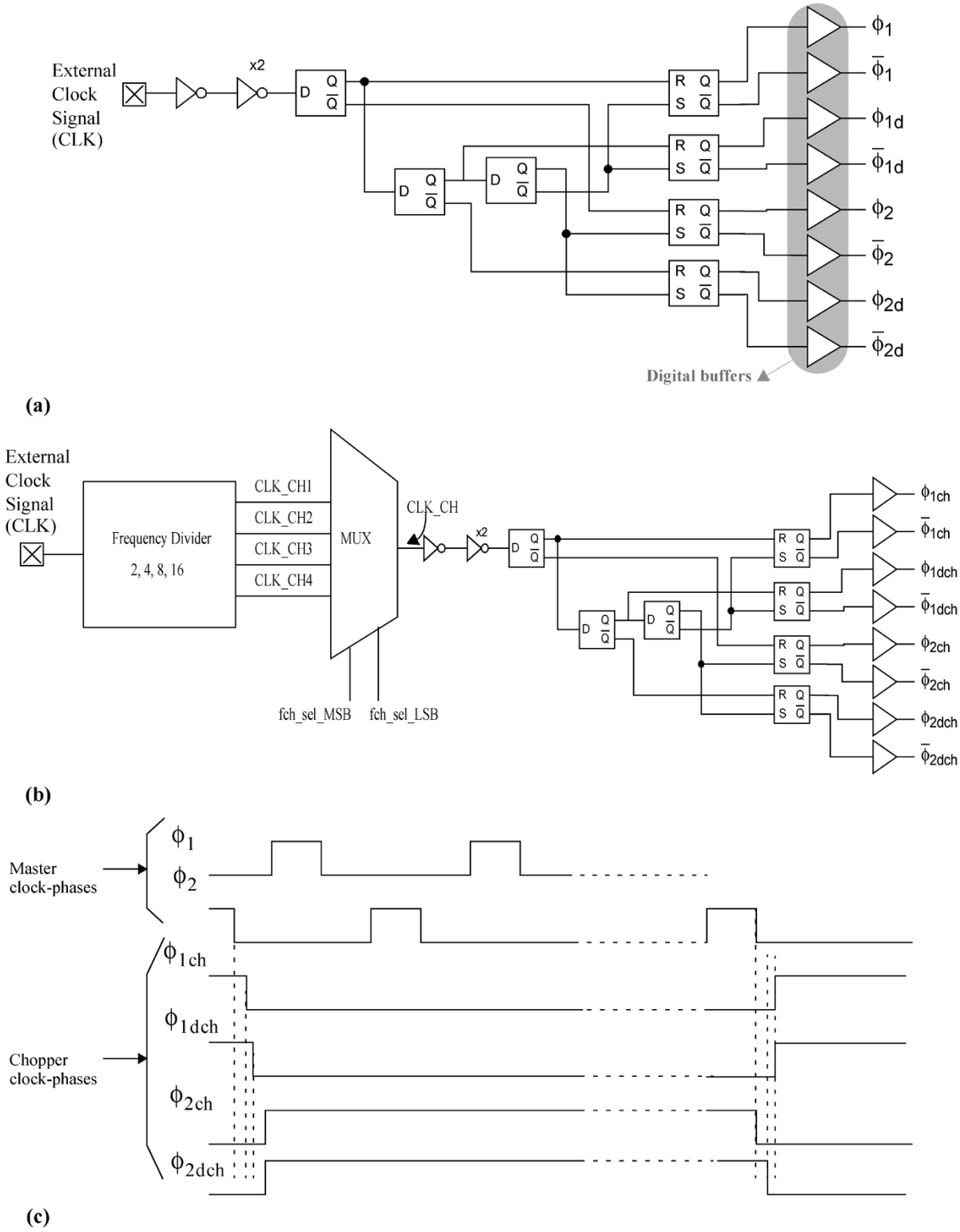



Fig. 13. Clock-phase generators: (a) master clock; (b) chopper clock; (c) clock-phase scheme.

supply and reference voltages. After the acquisition, which is automatically performed by controlling the test set-up through proprietary C routines, data were transferred to a workstation to perform the digital post-processing using MATLAB. The digital filtering was performed with a *Sinc* filter, implemented by software.

Fig. 16 shows a measured 65 536-point Kaiser-windowed FFT of the modulator output, clocked at 5 MHz and considering a −7-dBV, 5-kHz input sinewave, a modulator gain of $\xi = 1$, and a chopper frequency equal to $f_{\rm ch} = f_s/2$. The effect of varying the chopper frequency is illustrated in Fig. 17(a), which shows several output spectra corresponding

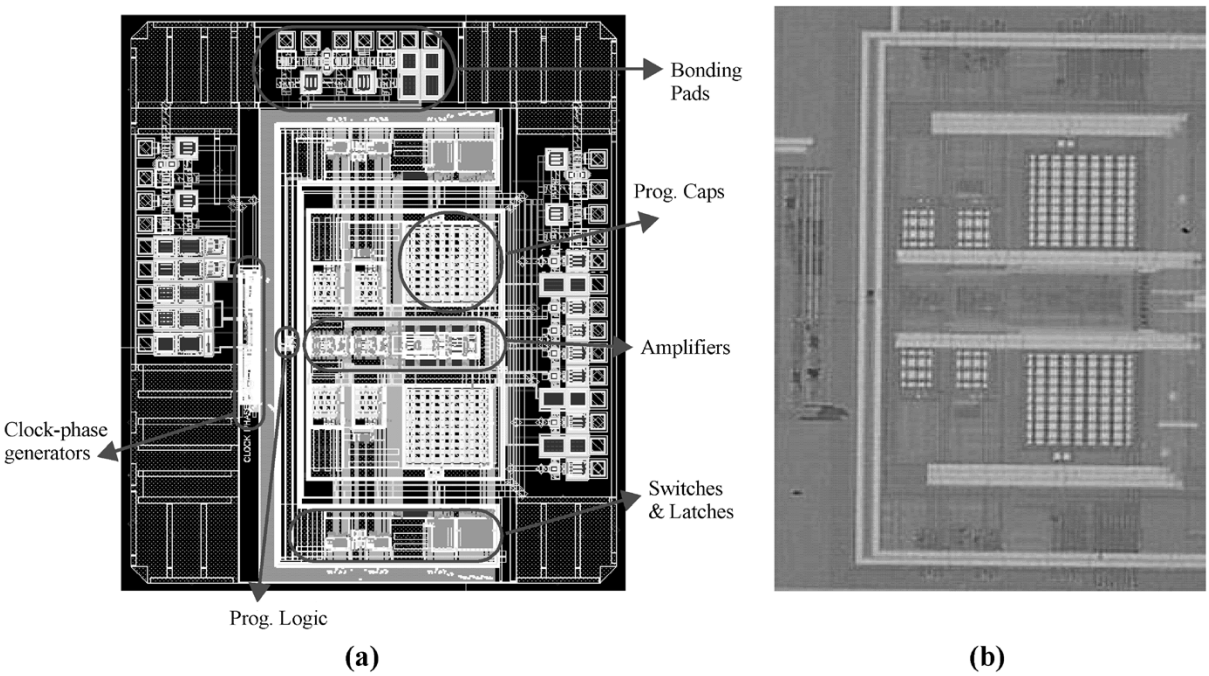



Fig. 14. (a) Complete layout of the modulator. (b) Microphotograph of the main parts of the chip.

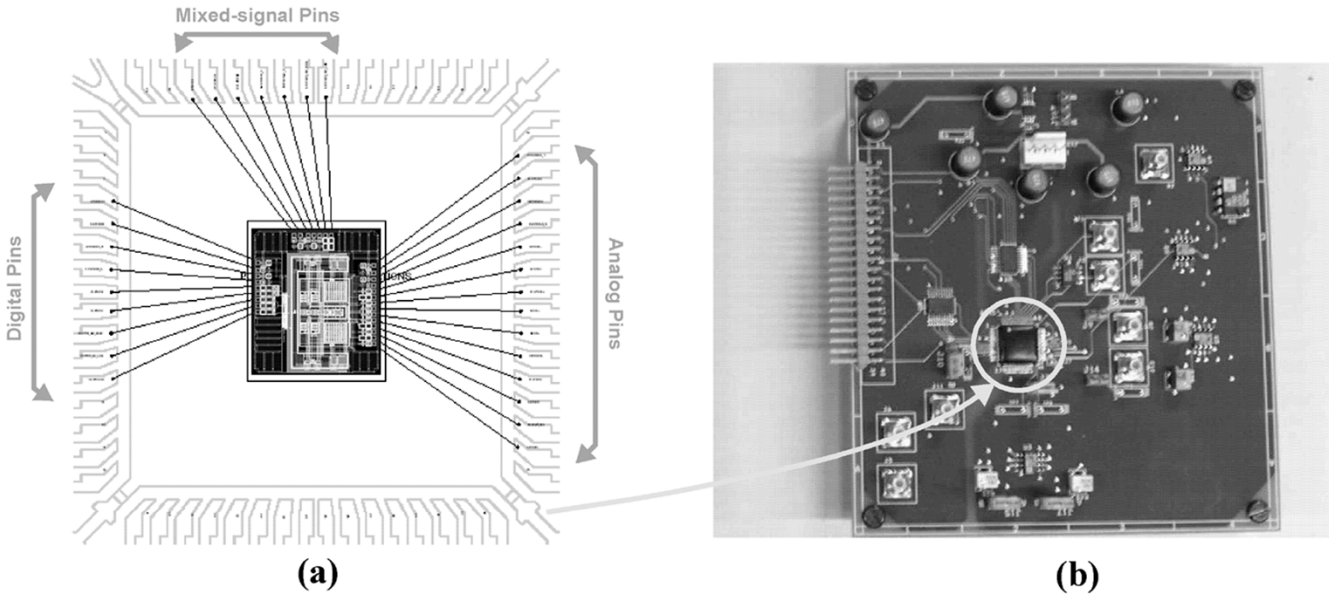



Fig. 15. (a) Bonding diagram of the $\Sigma\Delta$M chip and (b) PCB.

to $f_{\rm ch} = f_s/16, f_s/4, f_s/2$. Note that the lower $f_{\rm ch}$, the more flicker noise appears in the baseband, thus degrading the modulator performance. This is better illustrated in Fig. 17(b), where the signal-to-(noise + distortion) ratio (SNDR) versus the input signal amplitude is represented for $\xi = 1$ and different cases of $f_{\rm ch}$. It can be noted that the best performance is achieved for $f_{\rm ch} = f_s/2$. For that reason, all measurements are henceforth given for this value of $f_{\rm ch}$.

Fig. 18 shows several in-band (20-kHz) output spectra corresponding to the four different cases of the modulator gain ($\xi = 0.5, 1, 2, 4$) when a $-20$ dBV at 5 kHz input signal is applied. The measured in-band spectra are in good agreement with those obtained by behavioral simulation (see Fig. 7). Indeed, the measured in-band noise power is about $-96$ dB for each case of the modulator gain, corresponding to 16.2 bits with respect to the full-scale reference voltage. This resolution can be notably improved by the effect of the modulator gain. This is illustrated in Fig. 19 where the measured SNR and SNDR are represented against the input amplitude. The input-referred DR is approximately 104 dBV, i.e., 110 dB below the full-scale reference voltage ($V_{\rm ref} = 2$ V).

Note from Fig. 19 that in most cases of the modulator gain, the SNR/SNDR-peak is reached at approximately $-10$-dBFS signal amplitudes. Indeed, the in-band error power increases at those amplitudes as illustrated in Fig. 20. Behavioral simulations reveal that this nonlinear phenomenon is due to an incorrect oper-

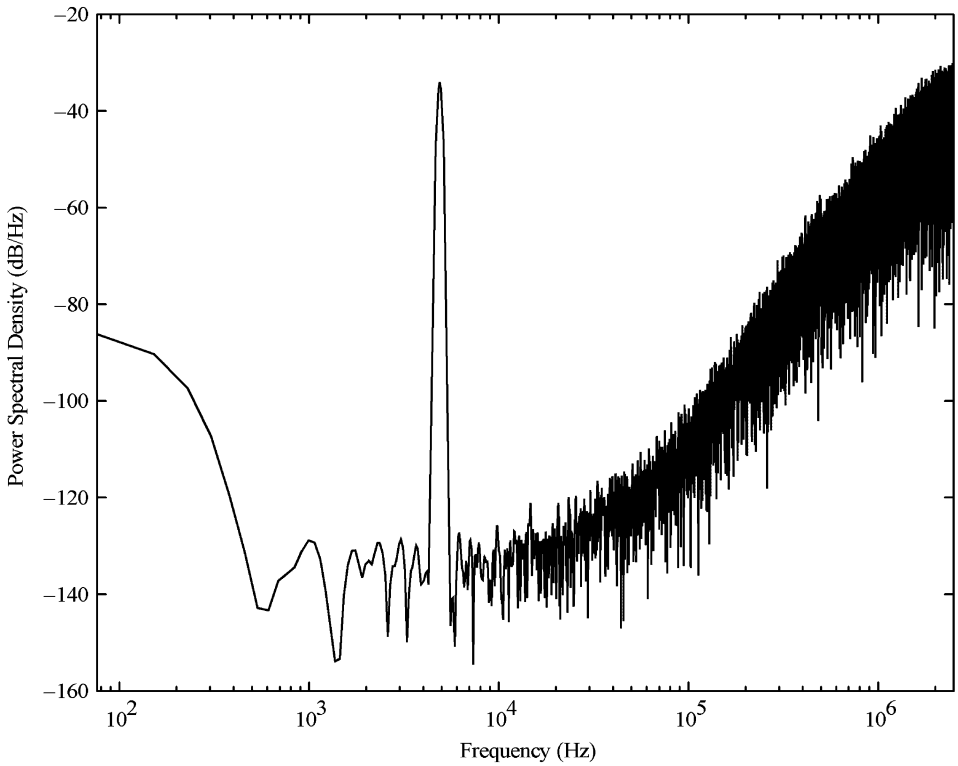



Fig. 16. Measured modulator output spectrum for a −7 dBV at 5-kHz input signal, $\xi = 1$ and $f_{\rm ch} = f_s/2$.

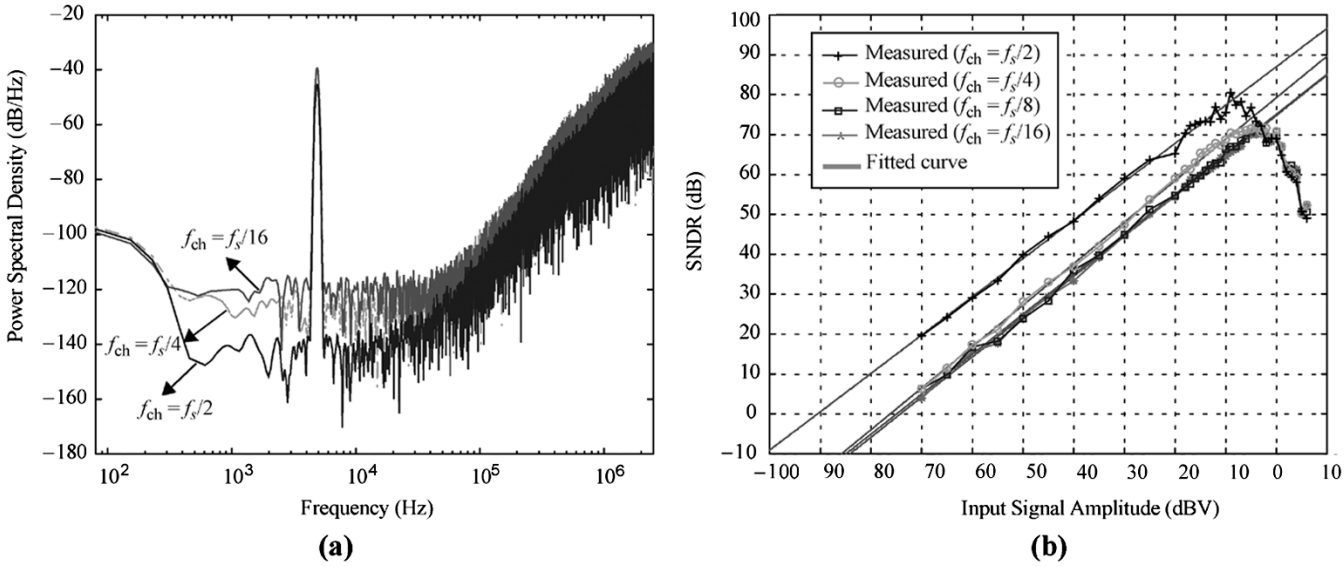



Fig. 17. Effect of chopper frequency on measured results: (a) Output spectra and (b) SNDR versus input signal amplitude for different cases of the chopper frequency $(f_{\rm ch})$.

ation of the chopper circuitry, which seems to be caused by the dielectric relaxation of the MIM capacitors in the first integrator [27]. This effect, often not properly characterized in most technology processes, may lead to an underestimation of the in-band noise power during the design phase, especially in high-resolution ADCs. Nevertheless, when the reference voltage is reduced from 2 V (nominal) to 1 V, the SNR peak improves in approximately 5 dB for all cases of the modulator gain, as illustrated in Fig. 21.

The noise-shaping is slightly degraded near the edge of the signal bandwidth, as illustrated in Figs. 16 and 18. Therefore, the performance near FS might be improved if a smaller signal bandwidth is taken. This is shown in Fig. 22 by plotting the SNR versus the input signal amplitude for different cases of the modulator gain and the reference voltage. Note that, in addition to the obvious resolution improvement due to doubling the oversampling ratio, the modulator behavior near FS is better than in Fig. 19.

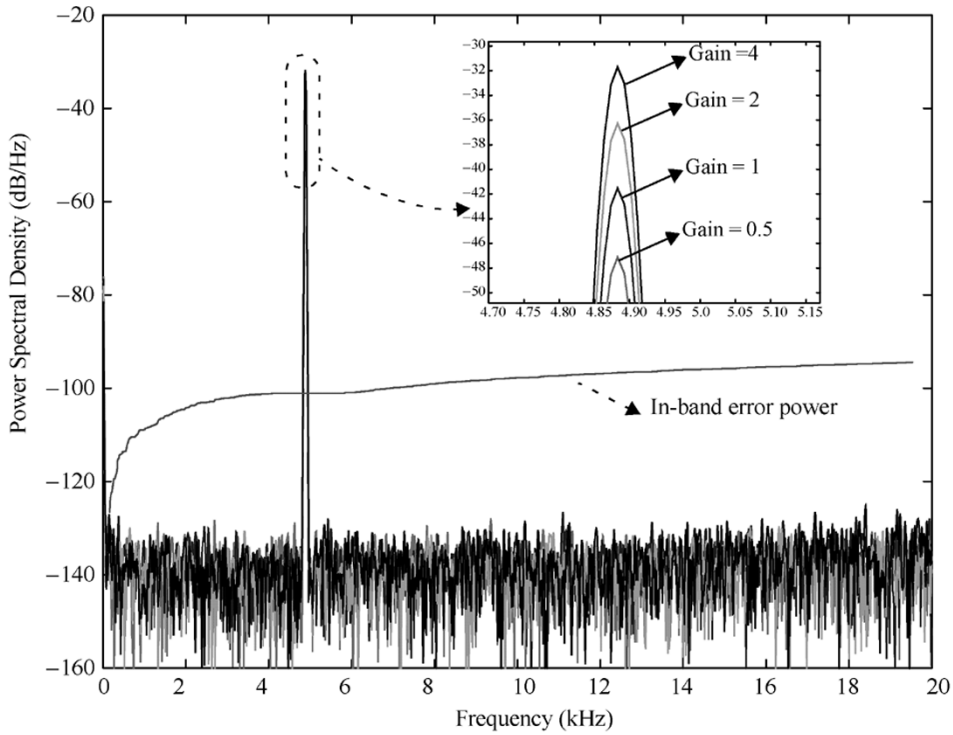



Fig. 18. Measured modulator in-band (20-kHz) spectra corresponding to the different gain cases.

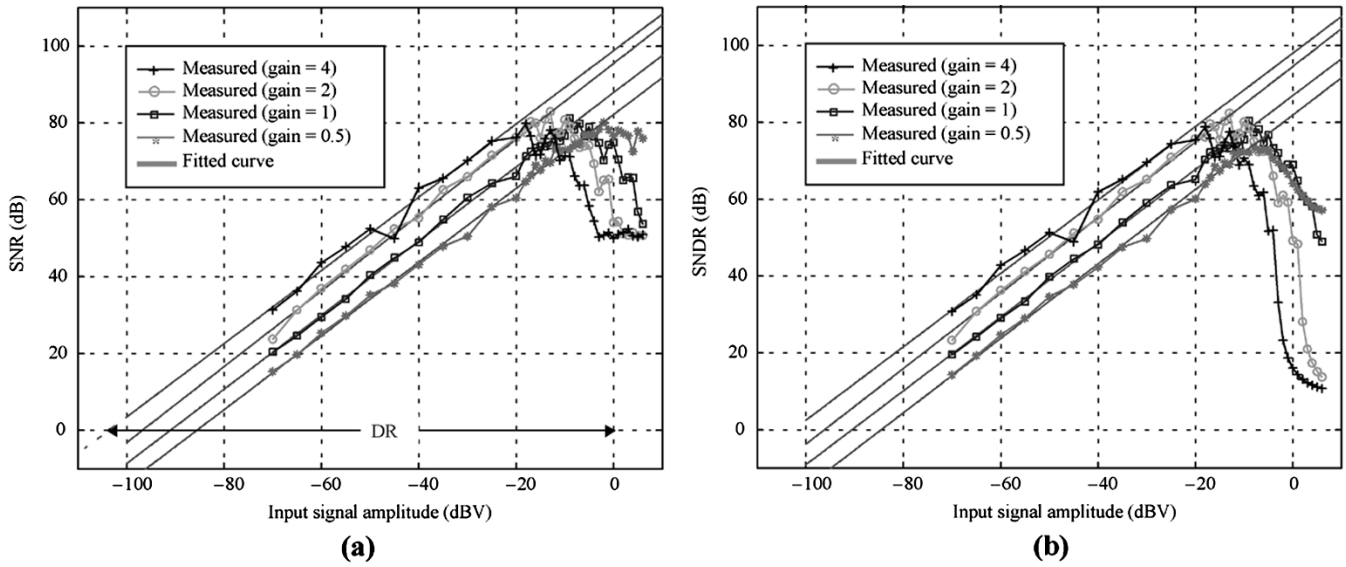



Fig. 19. (a) SNR and (b) SNDR as a function of the input amplitude for the different cases of modulator gain.

Table VIII summarizes the measured modulator performance by displaying its most significant figures. As a matter of conclusion, these features are compared in Fig. 23 with current state-of-the-art $\Sigma\Delta$Ms by using the following figure of merit (FOM) [10]:

$$\mathrm{FOM} = 2 \cdot 10^5 \cdot k \cdot T \cdot \frac{3 \cdot 2^{2 \cdot \mathrm{DRFS(bit)}} \cdot \mathrm{DOR(Hz)}}{\mathrm{Power(W)}} \qquad (6)$$

to quantify the quality of $\Sigma\Delta$Ms, where $\mathrm{DOR} = 2 \cdot B_w$ stands for the digital output rate. Note from (6) that the better the $\Sigma\Delta$M, the larger the value of FOM.

Table IX[6] compares the performance of those $\Sigma\Delta$Ms in Fig. 23 that achieve $\mathrm{FOM} > 200$. Note that, thanks to the combined use of modulator-gain programmability and high resolution,[7] the circuit in this paper achieves the largest FOM reported to date.

[6]All $\Sigma\Delta$Ms in Table IX use switched-capacitor techniques and achieve medium-high resolution within signal bandwidths below 25 kHz. Recently, continuous-time techniques are demonstrating to be very promising to achieve those resolutions in the MHz bandwidth [31].

[7]It is important to note that the dynamic range of the $\Sigma\Delta$M in this paper is enhanced by the action of the modulator gain programmability. This is one of the key features of the proposed modulator and it is very important for sensor applications in which there is a changing signal range. Note that if the unity-gain case is considered, the FOM decreases, being 25.4 for 20 kHz.

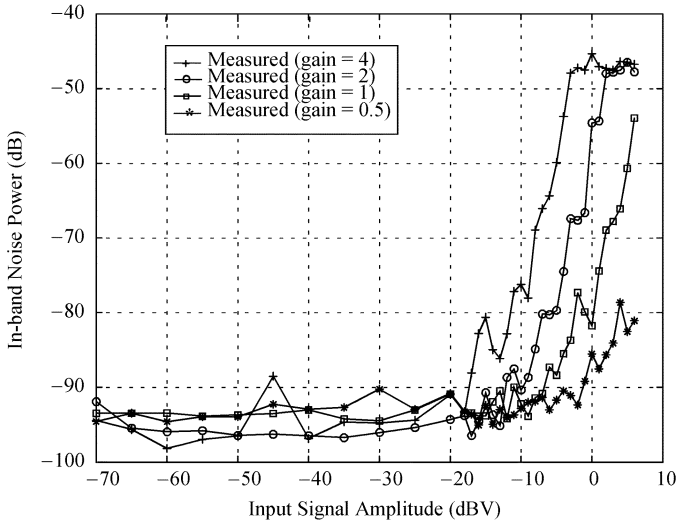



Fig. 20. In-band noise power as a function of the input signal amplitude.

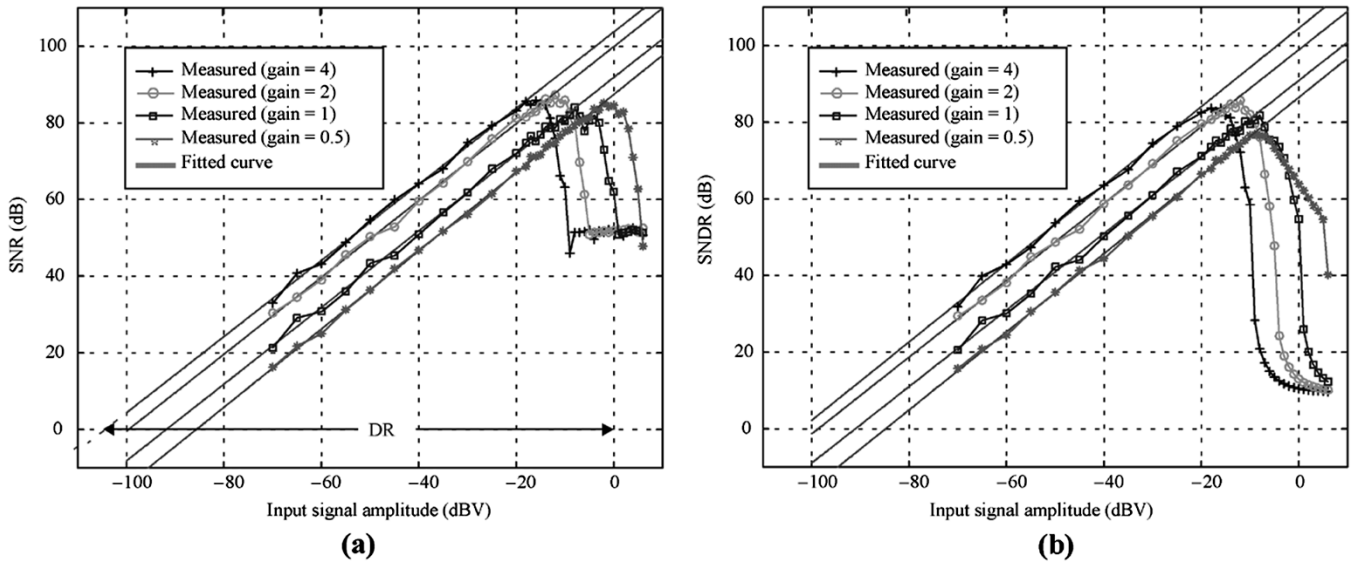



Fig. 21. (a) SNR and (b) SNDR as a function of the input amplitude for $V_{\rm ref} = 1$ V.

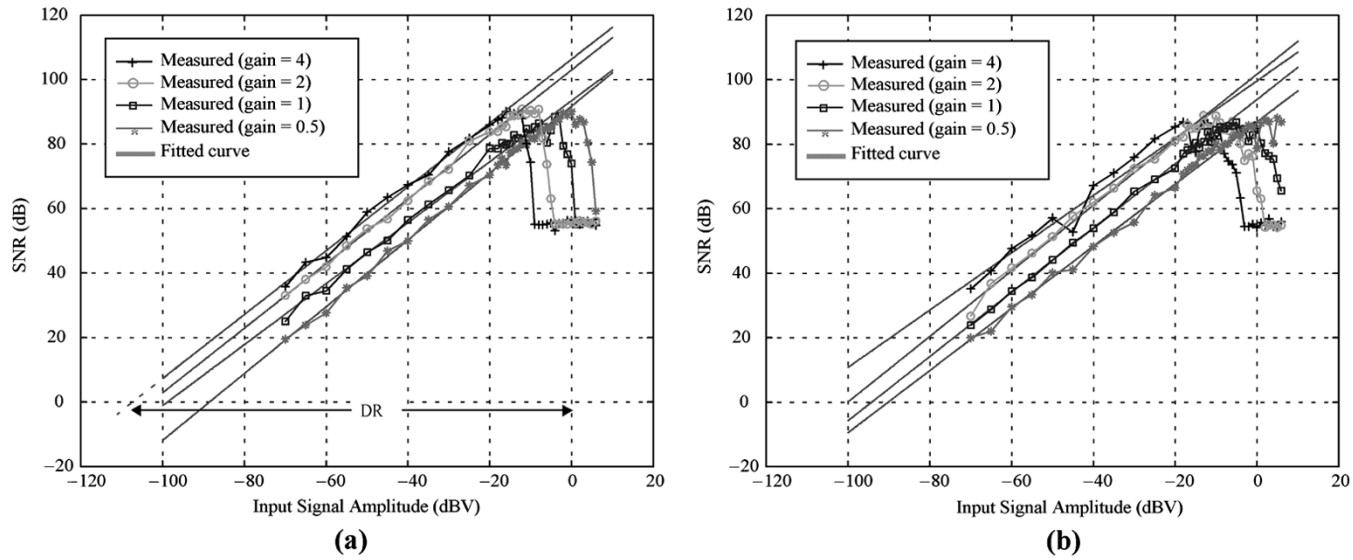



Fig. 22. SNR versus input amplitude for 10-kHz bandwidth: (a) $V_{\rm ref} = 1$ V; (b) $V_{\rm ref} = 2$ V.

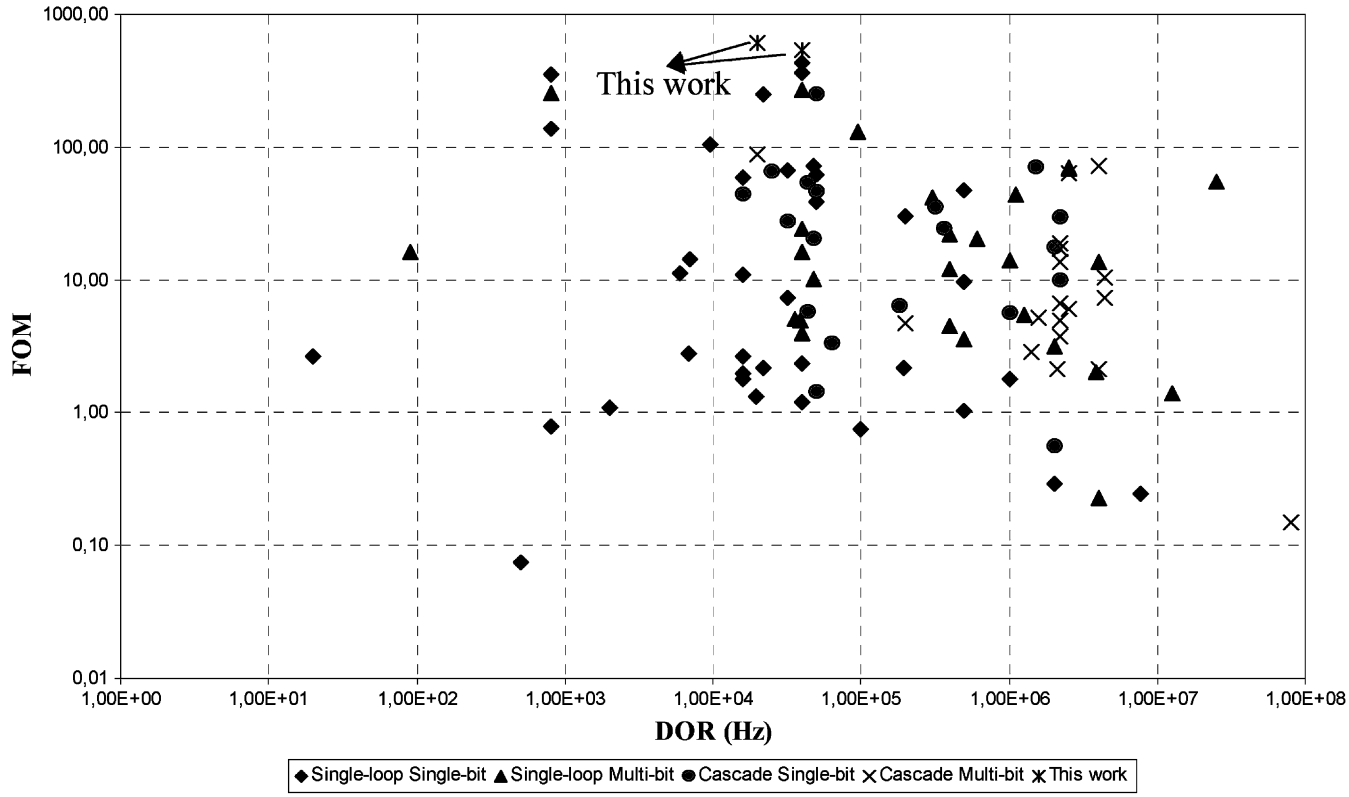



Fig. 23. Comparison with state-of-the-art ΣΔMs.

TABLE VIII
SUMMARY OF MEASURED PERFORMANCE

| | $V_{ref}$(V) | $B_w$ (kHz) | ξ | SNR/SNDR-peak[a] (dB) | DR (dBV)/ DRFS (dB) |
|---|---|---|---|---|---|
| Resolution/ Bandwidth | 2 | 20 | 0.5 | 80.2/73.5 | 85.1/91.6 |
| | | | 1 | 81.3/80.4 | 91.1/97.1 |
| | | | 2 | 82.9/82.5 | 96.9/102.9 |
| | | | 4 | 78.8/70.8 | 104.1/**110.1** |
| | | 10 | 0.5 | 88.0 | 90.3/96.3 |
| | | | 1 | 86.8 | 94.3/100.3 |
| | | | 2 | 89.0 | 100.1/106.1 |
| | | | 4 | 87.3 | 107.8/**113.8** |
| | 1 | 20 | 0.5 | 85.2/76.8 | 85.7 |
| | | | 1 | 84.0/81.8 | 91.9 |
| | | | 2 | 87.3/85.7 | 100.1 |
| | | | 4 | 85.8/83.7 | 104.1 |
| | | 10 | 0.5 | 88.5 | 90.1 |
| | | | 1 | 88.8 | 100.0 |
| | | | 2 | 90.7 | 103.0 |
| | | | 4 | 90.1 | 108.0 |
| Technology | 0.35μm 1P-5M CMOS | | | | |
| Architecture | Cascade 2-1 single-bit | | | | |
| Sampling Frequency | 5.12MHz | | | | |
| Active Area | 5.7mm$^2$ | | | | |
| Supply Voltage | 3.3V | | | | |
| Power Consumption | 14.7mW | | | | |

a. In the case of $B_w$ = 10kHz , measurements are given for a input signal frequency of 5-kHz and hence, only SNR is computed.

TABLE IX
PERFORMANCE COMPARISON ($\Sigma\Delta$Ms WITH FOM $> 200$)

| Author, year | DRFS (bits) | DOR (kS/s) | Power Consumption (mW) | FOM |
|---|---|---|---|---|
| Rabii, 1997 [10] | 16.1 | 50 | 2.5 | 246.3 |
| Snoeij, 2001 [28] | 16.7 | 22 | 2.5 | 248.9 |
| Nys, 1997 [29] | 19.0 | 0.8 | 2.18 | 252.4 |
| Yang, 2003 [11] | 18.7 | 40 | 68 | 266.3 |
| Kerth, 1994 [30] | 21.0 | 0.8 | 25 | 351.3 |
| Yao, 2004 [12] | 14.4 | 40 | 0.13 | 358.9 |
| Coban, 1999 [13] | 16.0 | 40 | 1 | 428.8 |
| This work | 18.1 | 40 | 14.7 | 536.1 |
| | 18.7 | 20 | | 615.9 |

## VI. CONCLUSION

A 0.35-$\mu$m CMOS programmable-gain cascade 2-1 $\Sigma\Delta$M to be included in an automotive sensor interface has been described. The main design considerations have been discussed and applied to select the most appropriate modulator architecture in terms of resolution, speed, and power consumption. The design of the prototype is based on a top-down CAD methodology that combines simulation and statistical optimization at different levels of the modulator hierarchy. Experimental results show that the dynamic range can be highly enhanced by the action of gain programmability. This combined effect places the presented chip at the cutting edge of state-of- the-art $\Sigma\Delta$Ms for similar applications, achieving the largest figure of merit reported up to now.

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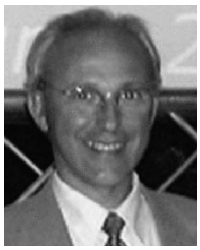

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