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GENERACIÓN Y EVALUACIÓN ON-CHIP DE SEÑALES  
ANALÓGICAS PARA APLICACIONES BIST DE CIRCUITOS  
ANALÓGICOS Y DE SEÑAL MIXTA

Memoria presentada por:  
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Para mi madre

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## Forewords and Acknowledgements

Before I started writing this thesis, a friend told me I should start writing the acknowledgements. It was a good advice, but I didn't. In case you are wondering, I started writing about signal characterization and the Fourier expansion, which, as you may imagine, are very impersonal topics. By the time I finished the whole document, I realized I didn't really want to write a single line more, but, honestly, the book you are holding right now wouldn't have been the same without the help of a number of people. I ought them this final effort.

Firstly, I would like to thank my supervisor Diego Vázquez for his advice and his patience in the endless discussions we had about the manuscript. I also want to thank Adoración Rueda for her guidance, and José Luis Huertas for being my first supervisor when I hadn't even finished my degree. I have to thank also the Spanish Government, which funded my work through the F.P.U. program.

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On the personal side, I want to thank my friends, for supporting me when I needed it most. I won't give any names. You know who you are.

Finally, I want to thank my family for being there. I wouldn't be the same without them.

Seville, 2009

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# TESIS



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En la actualidad, la rápida evolución de la capacidad de integración en tecnologías CMOS ha llevado a la industria de los circuitos integrados hacia sistemas complejos en los que coexisten bloques analógicos con componentes digitales [1]. Esto ha dado lugar a los, así llamados, SoCs (Sistemas on-chip, Systems on-Chip) en los que un sistema completo, compuesto de subsistemas analógicos, digitales y de señal mixta, es integrado sobre un mismo sustrato. Debido a este incremento en la complejidad, y a las restricciones de acceso a los nodos internos propias de los circuitos integrados, la labor de testar este tipo de sistemas se ha convertido en una componente importante en el coste de producción de un circuito integrado [2]-[5]. Coste que, además, no escala con el volumen de producción, como sería el caso, por ejemplo, de los equipos de test. Además, el problema del testado se complica a medida que crece la complejidad de la parte analógica del chip. Tanto es así que el test se está convirtiendo en un gran cuello de botella para la industria. De hecho, el SIA Roadmap for Semiconductors [2] identifica el test como uno de los problemas clave para la viabilidad económica de los futuros mercados de sistemas on-chip.

Testar un circuito integrado puede definirse como el proceso de verificar si éste cumple con las especificaciones para las que fue diseñado. Desde el punto de vista comercial, el test garantiza al posible comprador de un circuito integrado que las prestaciones del sistema se corresponden con la hoja de especificaciones que publica el vendedor. La opción obvia consiste en medir directamente el conjunto de especificaciones y comparar. Esta familia de test se conoce en la industria como test funcional. Otra opción consiste en localizar la presencia de defectos en el circuito. Dado que un circuito libre de defectos debe cumplir sus especificaciones por diseño, siempre dentro de las



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posibles variaciones del proceso, la detección de defectos es también una manera válida de garantizar su funcionalidad. Esta aproximación al test recibe el nombre de test estructural.

El test estructural está ampliamente aceptado en el test de circuitos digitales, en los que la comprobación directa de todas las posibles combinaciones de entrada y salida es prácticamente imposible dada la complejidad de los circuitos actuales. En esta línea, se han desarrollado modelos de fallos (como los modelos stuck-at) que permiten la identificación sencilla de defectos en el circuito, herramientas para la generación de patrones de test que maximizan la detección de estos fallos, e incluso existe un bus para test digital que se ha formalizado en los estándares IEEE 1149.1 e IEEE 1149.6 [14], [15].

La situación en el campo del test analógico y de señal mixta es completamente diferente. La industria suele preferir la medida directa de especificaciones sobre los modelos de fallo, y, además, estos modelos no están tan desarrollados en el plano analógico como en el caso digital. Tradicionalmente, el test de un sistema analógico se ha basado en test funcionales, en los que al circuito bajo test se le aplican ciertos estímulos y se analiza su respuesta para medir sus especificaciones. Sin embargo, los circuitos analógicos son muy sensibles a las condiciones de test como el ruido, los efectos de carga, variaciones de proceso, etc. lo que limita las posibilidades reales de monitorización y requiere en muchas ocasiones el empleo de costosos equipos de test (ATE, Automated Test Equipment) de alta precisión y velocidad.


Los esquemas de test BIST (autotest interno, Built-In Self-Test) son una posible solución a los problemas anteriormente citados. Las aproximaciones BIST consisten en trasladar total o parcialmente la funcionalidad de los ATEs (generación de estímulos de test, evaluación de la respuesta, control del test, etc.) al propio sistema bajo test. Un sistema BIST eficiente debe comprender los siguientes atributos:

- a) Interfaz digital de baja velocidad con el equipamiento de test externo dedicado a tareas de control y sincronización, de forma que sea posible el uso de ATEs digitales de bajo coste.
- b) Capacidad de programación para acomodar los estímulos de test a la medida.
- c) Robustez frente a ruido y variaciones de proceso.
- d) Bajo esfuerzo de diseño y bajo impacto en el área total del sistema.

Es claro que tal sistema representa una disminución importante del coste asociado al test respecto a estrategias de testado tradicionales. Esta tesis está centrada en el marco de las aplicaciones BIST para circuitos analógicos y de señal mixta. En particular, los trabajos realizados y que aquí se exponen se han dirigido a la obtención y desarrollo de nuevos métodos on-chip para la generación y caracterización de señales de test analógicas periódicas, que cumplan con los atributos anteriormente expuestos para sistemas BIST. Cada bloque por separado tiene un innegable potencial de aplicación en el campo del test analógico y de señal mixta, dado que la mayoría de estos sistemas pueden ser testados y/o caracterizados mediante la aplicación de un estímulo periódico, usualmente sinusoidal,



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y el análisis de la señal de respuesta a ese estímulo. Bloques básicos como filtros, acondicionadores de señal, convertidores analógico-digital y digital-analógico, etc. Además, la caracterización de señales periódicas es también un punto clave para ciertos esquemas de test estructural, como es el test basado en oscilación (OBT, Oscillation-Based Test) [71]-[75].

Esta tesis está organizada en las siguientes secciones:

En la sección 1 se propone un nuevo método de generación de señales analógicas periódicas que resulta muy adecuado para su inclusión en técnicas BIST dado su simplicidad y robustez, mientras que mantiene los atributos de control digital y programabilidad. La viabilidad del sistema propuesto se verifica mediante el desarrollo y validación experimental de dos prototipos integrados.

En la sección 2 se presenta una metodología novedosa para la caracterización completa de una señal periódica analógica que es fácilmente implementable on-chip. La discusión se completa con el desarrollo de un prototipo integrado y su caracterización en el laboratorio.

La sección 3 presenta una aplicación particular en la que se emplean ambos bloques de test para componer un analizador de redes/espectros. El sistema se ha construido sobre una placa de test y se ha empleado para la caracterización de un filtro analógico a modo de ejemplo de funcionamiento.

Finalmente, la sección 4 resume las principales conclusiones que se derivan de los trabajos presentados.

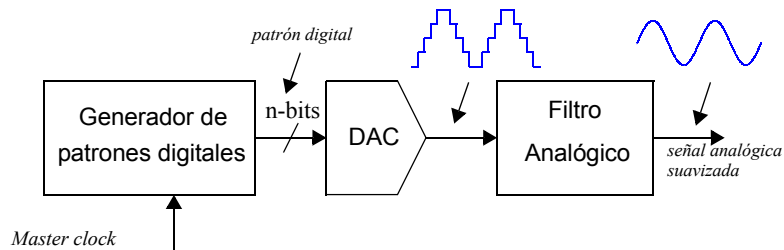
## **1. Generación de señales sinusoidales analógicas para aplicaciones BIST**

Los esquemas de test funcionales para circuitos analógicos y de señal mixta hacen uso de generadores de señal para proporcionar estímulos de test. Señales tales como rampas, sinusoides, ondas triangulares, etc, son algunos ejemplos de señales analógicas ampliamente usadas como estímulo en diferentes estrategias de test. Esta sección se centra en la generación on-chip de señales sinusoidales. Este tipo de señales presenta un especial atractivo en el marco de esta tesis debido a su gran potencial de aplicación en el test de sistemas analógicos y señal mixta.

### **1.1. Revisión de técnicas anteriores**

Una solución clásica para la generación on-chip de señales sinusoidales es el uso de osciladores [41]-[44]. Un oscilador consiste en una etapa de filtrado con un mecanismo de realimentación no lineal. Este último fuerza la oscilación mientras que el filtro elimina las componentes armónicas no

**FIGURA 1. Generador de señales analógicas basado en técnicas digitales**



deseadas. La calidad de la señal generada depende en gran medida de la característica no lineal del mecanismo de realimentación y de lo selectivo que sea el filtro.

Otras aproximaciones adaptan soluciones digitales usando el esquema de la Figura 1. La implementación directa de este esquema usando elementos de memoria como generador digital generalmente no es práctica. A menos que los elementos de memoria estén ya incluidos en el sistema y puedan ser reutilizados, esta aproximación representa un gran incremento del área del sistema.

Los trabajos en [45],[46],[48]-[50] explotan las propiedades de conformación de ruido de la modulación  $\Sigma\Delta$ . Estos generadores se basan en la generación de una secuencia de bits que codifica a una señal sinusoidal empleando modulación  $\Sigma\Delta$ . Filtrando convenientemente esta secuencia, se consigue eliminar el ruido de cuantización y reconstruir la señal analógica. Este método es válido para señales monotonales y multitonales y ofrece grandes ventajas en términos de simplicidad y robustez, ya que la circuitería empleada es en su mayor parte digital. Sin embargo este esquema de generación requiere secuencias digitales largas para controlar la amplitud y la frecuencia de la señal generada, y un filtro de salida selectivo (al menos un orden mayor que el orden de la modulación  $\Sigma\Delta$  empleada) para eliminar el ruido de cuantización.

Los trabajos en [51]-[52] presentan una solución muy sencilla para la generación de señales analógicas periódicas de tiempo discreto. Esta técnica de generación se basa en un amplificador de ganancia variable (VGA, variable gain amplifier) de capacidades conmutadas (SC, Switched Capacitor) cuya ganancia varía de forma escalonada siguiendo la evolución de una senoide. Esta aproximación es en realidad muy parecida al diagrama general en la Figura 1, si se tiene en cuenta que el VGA con su control digital de la ganancia juega el papel del convertidor D/A. En el caso de señales sinusoidales, sólo  $N/4+1$  pasos de ganancia son necesarios para generar una señal con  $N$  escalones por periodo, si  $N$  es potencia de 2. Las principales ventajas de esta aproximación son que tanto la amplitud como la frecuencia de la señal generada pueden controlarse fácilmente mediante una tensión de DC a la entrada y la frecuencia de reloj, respectivamente, junto con la simplicidad y

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robustez inherente a la lógica y la circuitería SC empleadas. La calidad espectral de la señal generada en términos de SFDR y THD (Spurious-Free Dynamic Range y Total Harmonic Distortion, respectivamente) está limitada en este caso por la exactitud de los escalones generados y su número. El número de escalones debe mantenerse bajo, porque si no es así, el área puede incrementarse drásticamente. Mejorar las prestaciones pasa por el uso de una etapa de filtrado a la salida que elimine las componentes armónicas no deseadas de la señal.

## 1.2. Estrategia propuesta para la generación de señales sinusoidales

En todas las aproximaciones anteriormente presentadas, es necesario el empleo de un filtro analógico a la salida para reconstruir o suavizar la señal sinusoidal. Nuestra propuesta en este trabajo es incluir la generación de la señal en el propio filtro. La idea es extender el esquema en [51] fundiendo la generación de señal y el filtrado de las componentes no deseadas en el propio filtro de salida, mediante el empleo de un filtro modificado convenientemente. Esta aproximación mantiene los atributos de control digital, programabilidad y robustez, y además reduce significativamente los requerimientos de área.

### 1.2.1. Base teórica

Primeramente, es conveniente destacar que aunque la discusión se restringirá al dominio continuo, ésta puede ser directamente extendida al caso discreto.

Sea un sistema lineal de orden  $n$  con una entrada,  $u(t)$ , y una salida,  $y(t)$ , descrito en términos de sus variables de estado,  $[x(t)]$ , en la forma,

$$\begin{aligned} [\dot{x}(t)] &= [a][x(t)] + [b(t)]u(t) \\ y(t) &= [c][x(t)] + d(t)u(t) \end{aligned} \quad (1)$$

donde  $[x(t)]$  es el vector columna  $n \times 1$  de las variables de estado, el coeficiente  $[a]$  es una matriz  $n \times n$ , el coeficiente  $[b(t)]$  es un vector columna  $n \times 1$ , el coeficiente  $[c]$  es un vector fila  $1 \times n$ , y el coeficiente  $d(t)$  es una función escalar. Los coeficientes  $[b(t)]$  y  $d(t)$ , que relacionan la entrada del filtro con la evolución de las variables de estado y con la salida del filtro son variantes en el tiempo.

Consideremos el caso particular  $[b(t)] = [b]f(t)$  y  $d(t) = df(t)$ , donde  $[b]$  y  $d$  son constantes y  $f(t)$  es una función dependiente del tiempo. En este caso, usando la transformada de Laplace es fácil resolver el sistema,

$$\begin{aligned} Y(s) &= H(s)\{F(s) \otimes U(s)\} \\ y(t) &= h(t) \otimes \{f(t)u(t)\} \end{aligned} \quad (2)$$

donde las mayúsculas denotan la transformada de Laplace, el operador  $\otimes$  representa el producto de convolución,  $H(s)$  es una función de transferencia, dada por,

$$H(s) = [c]\{s[I] - [a]\}^{-1}[b] + d, \quad (3)$$

$[I]$  es la matriz identidad  $n \times n$ , y  $h(t)$  es la transformada inversa de Laplace de  $H(s)$ .

De (2) es fácil deducir que el sistema realiza, en el caso más general, el filtrado del producto  $f(t)u(t)$ . Es decir, el sistema actúa como un filtro y un multiplicador, todo en uno. Restringiéndonos a su uso como generador de señal (el uso como multiplicador, aunque interesante, está fuera del objeto de este trabajo) consideremos el caso particular  $u(t) = u$ , donde  $u$  es una constante. Entonces, la salida del sistema se puede reescribir como,

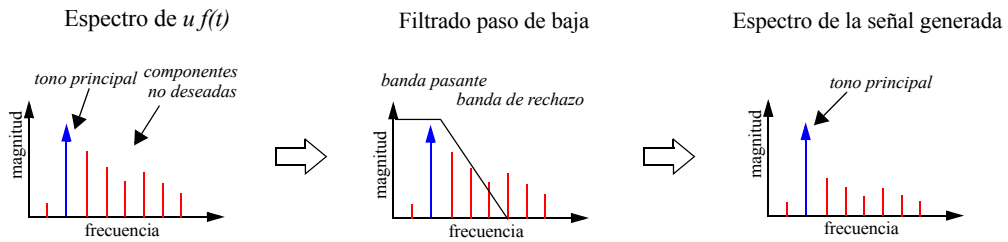
$$\begin{aligned} y(t) &= h(t) \otimes \{u \cdot f(t)\} = u \cdot \{h(t) \otimes f(t)\} \\ Y(s) &= uH(s)F(s) \end{aligned} \quad (4)$$

La respuesta del sistema es equivalente a la de un filtro lineal con función de transferencia  $H(s)$  excitado por una señal  $u \cdot f(t)$ . Es claro que si  $f(t)$  es una función periódica, la respuesta del sistema también será una señal periódica. Respecto a la generación de señales sinusoidales, básicamente cualquier función periódica  $f(t)$  puede ser apropiada para este propósito, dada una función de transferencia  $H(s)$  lo suficientemente selectiva como para atenuar todas las componentes espectrales no deseadas, como se ilustra en la Figura 2 usando un filtro paso de baja como ejemplo.

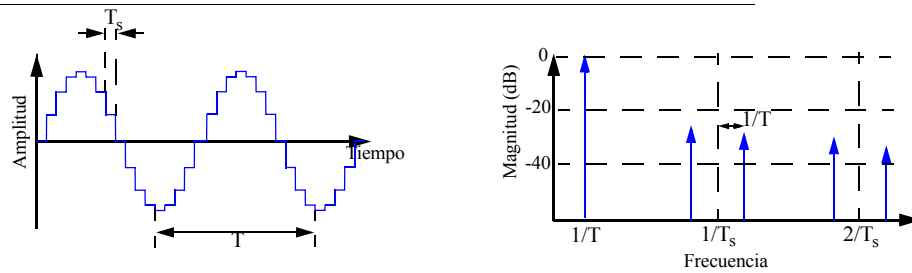
Es importante destacar que la amplitud y la frecuencia de la señal generada son controladas de manera sencilla. La amplitud a través del factor de escala  $u$ , mientras que la función  $f(t)$ , junto al sintonizado adecuado de la función de transferencia del sistema, se puede usar para controlar su frecuencia.

En relación a la elección de la función  $f(t)$ , ésta puede tener diversas formas. Cualquier función periódica puede ser adecuada desde un punto de vista teórico. No obstante, la elección de  $f(t)$  debe ser dirigida principalmente por dos factores: su facilidad de implementación dentro del propio filtro y la magnitud de las componentes espectrales no deseadas que puede introducir. Una buena solución de compromiso consiste en implementar  $f(t)$  como una senoide escalonada, como se muestra en la Figura 3. El espectro de esta señal es esencialmente el espectro de una senoide muestreada idealmente, pero modulado por una función sampling. Además, debido a la simetría de las señales sinusoidales, si el número de niveles por periodo,  $N$ , es una potencia de 2, sólo  $N/4+1$  niveles diferentes describen la forma de onda completa. Desde el punto de vista de la implementación, es sencillo ver que dicha función se puede construir fácilmente conmutando los dispositivos de entrada del sistema.

**FIGURA 2. Generación de una señal sinusoidal a partir del tono principal de  $f(t)$  con un filtrado paso de baja**



**FIGURA 3. Sinusoide escalonada ideal**



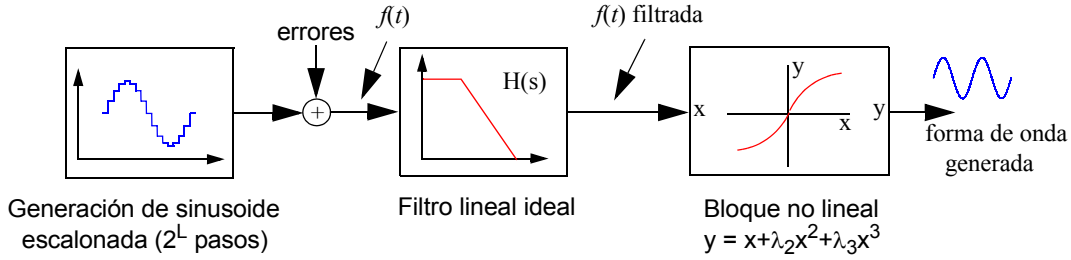
### 1.2.2. Consideraciones de alto nivel

En esta sección pretendemos hacer un estudio de las limitaciones de la técnica de generación propuesta. Para ello, es necesario hacer algunas consideraciones para ser realistas en el análisis.

Las principales limitaciones que presenta nuestra aproximación vienen dadas por:

- La realización de la función  $f(t)$ : restringiendo la discusión a funciones sinusoidales escalonadas, las prestaciones del generador se verán afectadas tanto por el número de escalones por periodo como por los posibles errores que pueden afectar al nivel de cada escalón.
- El sistema lineal escogido: la forma de la función de transferencia  $H(s)$  define la atenuación de las componentes no deseadas de la función  $f(t)$ , mientras que sus no idealidades en términos de comportamiento no lineal, distorsionará la señal de salida.

**FIGURA 4. Modelo de alto nivel para el esquema de generación propuesto**



La Figura 4 muestra un modelo de alto nivel que contempla estas limitaciones. El modelo consiste en tres bloques principales: un bloque de entrada que genera la función  $f(t)$  (por simplicidad se ha supuesto que  $u$  es unidad), un filtro ideal con función de transferencia  $H(s)$ , y un bloque no lineal que modela la no linealidad del filtro.

Con respecto a  $f(t)$ , ésta estará compuesta por  $N$  escalones por periodo (siendo  $N$  par), de duración  $T_s$  (véase la Figura 3). Tanto el número de escalones por periodo como los posibles errores que pueden afectar al nivel de cada escalón tienen un impacto directo en las prestaciones del sistema.

Por una parte, existe un compromiso entre el número de niveles y el orden del filtro. Así, un número alto de escalones por periodo empujaría las réplicas espectrales a frecuencias altas, relajando las especificaciones del filtro, pero complicando la realización de la función  $f(t)$ . En cambio, un número bajo de escalones reduce la complejidad de  $f(t)$ , pero requiere un filtro más selectivo para atenuar las réplicas.

Por otra parte, el nivel de cada escalón puede estar afectado por errores, que, desde el punto de vista de la implementación, pueden ser debidos a desapareamiento entre los dispositivos de entrada del filtro, variaciones del proceso, variaciones en las alimentaciones, etc. Estas variaciones introducen errores,  $\varepsilon_i$ , en los niveles de la función  $f(t)$ . En términos espectrales, esto hace que el espectro de  $f(t)$  esté compuesto por un tono principal a frecuencia  $1/NT_s$ , armónicos no deseados debido a los errores a los múltiplos de esa frecuencia,  $k/NT_s$ ,  $k=2, 3, \dots$ , y réplicas del espectro alrededor de las frecuencias  $mT_s$ ,  $m=1, 2, \dots$ , todo ello modulado por la función sampling  $|S_a(\omega T_s/2)|$ .

Con respecto al filtro, consideramos los casos de primer y segundo orden, paso de baja y paso de banda. El efecto de un filtro de orden mayor puede ser derivado a partir de ellos. Los filtros paso de baja de primer orden y paso de baja y paso de banda de segundo orden están descritos por sus funciones de transferencia:

$$H_1^{LP}(s) = \frac{k}{1 + s/\omega_0}, \quad (5)$$

$$H_2^{LP}(s) = \frac{k\omega_0^2}{s^2 + (\omega_0/Q)s + \omega_0^2}, \quad (6)$$

$$H_2^{BP}(s) = \frac{k(\omega_0/Q)s}{s^2 + (\omega_0/Q)s + \omega_0^2}, \quad (7)$$

respectivamente, donde  $k$  es un factor de escala,  $\omega_0$  es la frecuencia angular del polo (o de los polos) y  $Q$  es el factor de calidad de los polos (asumiendo que estos son complejos conjugados).

El objetivo es colocar las componentes armónicas no deseadas de  $f(t)$  en la banda de rechazo, mientras que el armónico principal se mantiene en la banda pasante. La mejor elección para este propósito es claramente hacer,

$$\omega_0 = \frac{2\pi}{NT_s} \quad (8)$$

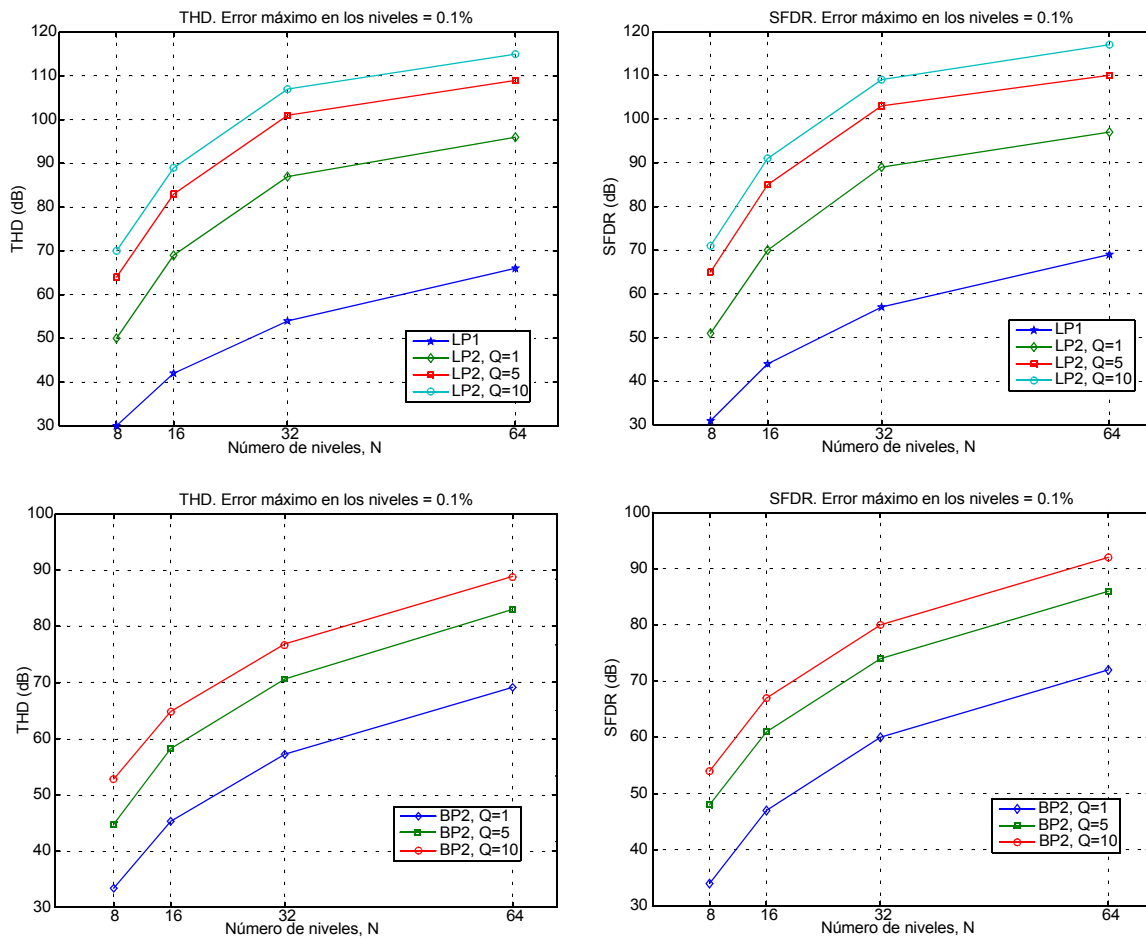
donde  $\omega_0$  es la frecuencia del polo (o de los polos en el caso de segundo orden), dado que así la componente principal de la señal estará cerca del pico de ganancia del filtro (si el factor de calidad  $Q$ , en el caso de sistemas de segundo orden, es  $Q > 1/2$ ) mientras que los armónicos estarán en la banda de rechazo y serán atenuados por el filtro.

Para estimar los efectos del filtrado sobre  $f(t)$  se ha realizado un análisis de Monte Carlo usando errores máximos para los niveles del 0.1% y del 1% y aplicando las etapas de filtrado anteriormente mencionadas con diferentes valores de  $Q$  para los filtros de segundo orden. La Figura 5 muestra los peores casos obtenidos en términos de SFDR y THD para un error máximo de 0.1% en los niveles, y para diferentes valores del factor de calidad  $Q$ . Por otra parte, la Figura 6 muestra los peores casos para  $Q=5$  como función del número de niveles y su error máximo.

Es claro ver como para un bajo número de niveles, las prestaciones obtenidas están limitadas principalmente por la primera réplica espectral, siendo muy insensible a los errores de los niveles, mientras que a partir de  $N > 16$ , el efecto de las réplicas puede ser despreciado y son los errores en los niveles los que limitan las prestaciones del sistema.

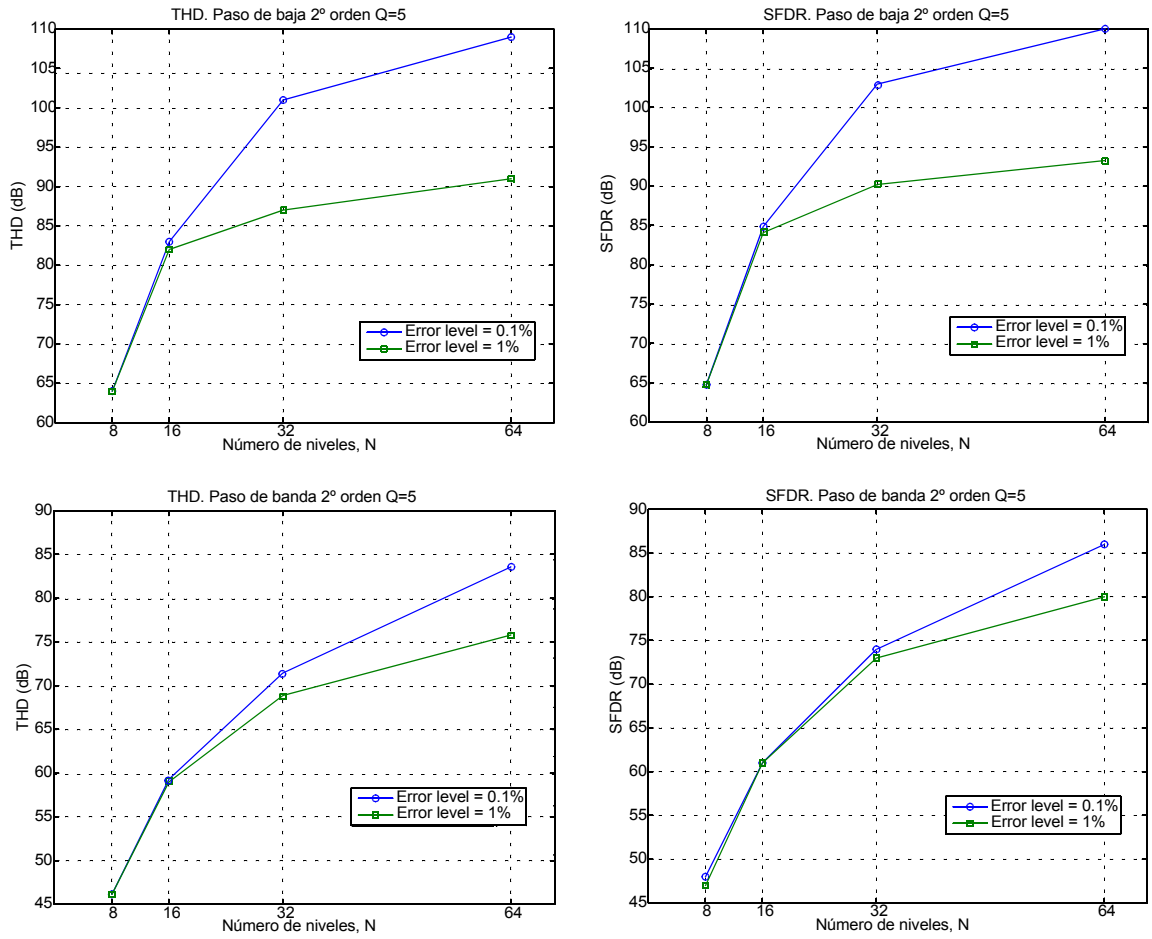
Los resultados obtenidos muestran que se pueden obtener valores altos de THD y SFDR con un bajo número de niveles y un filtro de bajo orden. Por ejemplo, se obtienen valores alrededor de 80dB para THD y SFDR con  $N=16$  y  $Q=10$  con un error en los niveles del 1% y un filtro paso de baja de segundo orden.

**FIGURA 5. Estimaciones de SFDR y THD para un error máximo en los niveles del 0.1% y diferentes valores de  $Q$**





**FIGURA 6. Estimaciones de SFDR y THD para  $Q=5$  y diferentes valores del error máximo en los niveles**



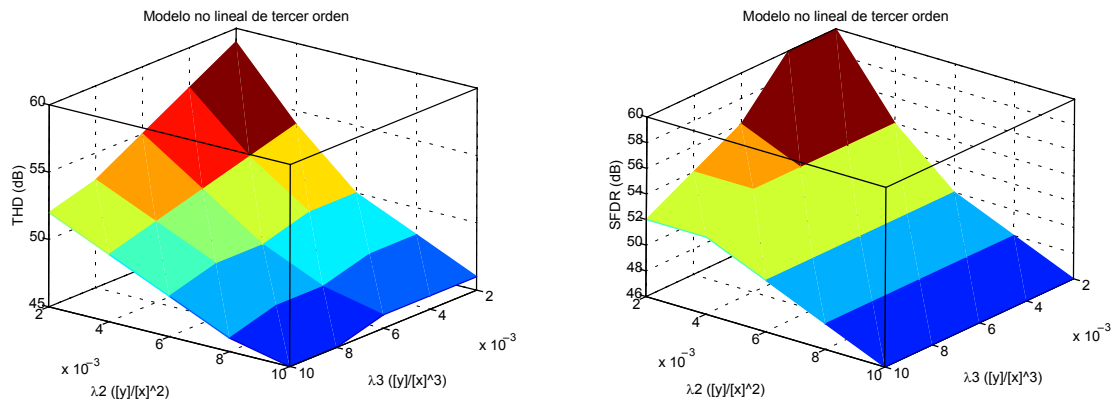
Para poner los resultados obtenidos en perspectiva se puede hacer una comparación con otras técnicas de generación. Por ejemplo, si se usa la estrategia de generación basada en modulación  $\Sigma\Delta$  usando un registro de 200 bits y un filtrado ideal de tercer orden sobre una secuencia optimizada codificada con una modulación  $\Sigma\Delta$  de segundo orden, se obtienen aproximadamente 75dB y 72dB de SFDR y THD, respectivamente, aunque los peores casos debido a pequeñas variaciones de los parámetros de la señal codificada (como amplitud o fase) pueden resultar en una caída significativa en las prestaciones, por debajo de 50dB en términos de THD y SFDR [50]. Nótese que la no linealidad del filtro no se ha considerado en la comparación, ya que afectaría del mismo modo a ambas aproximaciones. Para igualar los resultados obtenidos con la técnica de generación propuesta usando esta estrategia basada en modulación  $\Sigma\Delta$ , sería necesario usar secuencias digitales más largas, es decir, un registro más largo, un filtro de orden superior, o una combinación de ambos. Sin embargo estos resultados son optimistas, en el sentido de que la no linealidad del propio filtro no ha sido considerada aún en el análisis.

Con respecto a la no linealidad del filtro, ésta depende fuertemente del tipo de filtro particular empleado, su estructura y su topología de circuito. Sin embargo, el efecto de la no-linealidad puede ser modelado fácilmente por el bloque no lineal introducido en la Figura 4. En general, la característica no lineal de un filtro puede ser modelada por un polinomio de la forma,

$$y(t) \approx x(t) + \lambda_2 x^2(t) + \lambda_3 x^3(t) + \dots \quad (9)$$

donde  $x(t)$  representa la salida del filtrado ideal, los coeficientes  $\lambda_i$  modelan la característica no lineal del filtro e  $y(t)$  es la salida del sistema. Normalmente, un polinomio de tercer grado es suficiente para el modelo, aunque polinomios de orden mayor pueden usarse para sistemas fuertemente no lineales.

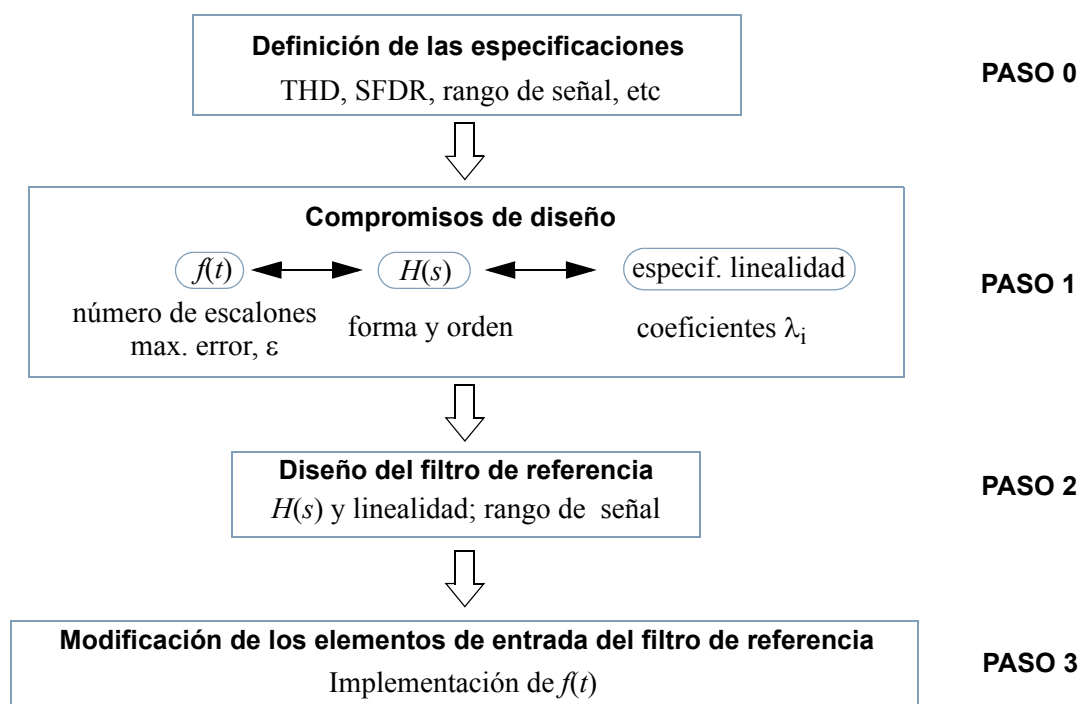
**FIGURA 7. Estimaciones de THD y SFDR producidos por un modelo de tercer orden**



La Figura 7 muestra el THD y SFDR introducidos por (9), obtenidos con un modelo de tercer grado para diferentes valores de los coeficientes  $\lambda_2$  y  $\lambda_3$  cuando  $x(t)$  es una senoide ideal.

El modelo de alto nivel discutido se puede usar para guiar el proceso de diseño del generador. En realidad, define una metodología de diseño, que se ha representado en el diagrama de flujo mostrado en la Figura 8. Una vez definido el conjunto de especificaciones del generador que se pretende diseñar, primeramente se considera el compromiso entre la elección de  $f(t)$ ,  $H(s)$ , y las especificaciones de linealidad. El modelo de alto nivel presentado es muy útil en esta etapa. El siguiente paso consiste en proponer una arquitectura de filtro particular compatible con la función de transferencia  $H(s)$  y con las especificaciones de linealidad obtenidas en el paso anterior. Para completar el diseño del generador basta modificar los elementos de entrada del filtro para implementar la función  $f(t)$  definida anteriormente. El flujo de diseño es muy parecido al diseño de un filtro analógico, a excepción del último paso en el que se modifican los elementos de entrada de éste.

**FIGURA 8. Flujo de diseño conceptual para el generador propuesto**



### 1.3. Prototipos integrados

La técnica de generación desarrollada se reduce a un simple filtro analógico de bajo orden que incluye elementos de entrada variables en el tiempo. En esta sección se presenta el diseño de dos prototipos demostradores del esquema de generación propuesto. En concreto se han desarrollado dos generadores: uno basado en un filtro OTA-C de segundo orden y otro basado en un filtro SC de segundo orden, usando en ambos casos una tecnología CMOS estándar de  $0.35\mu\text{m}$ .

En ambos casos la función  $f(t)$  que describe la variación de los elementos de entrada del filtro es una función sinusoidal escalonada con 16 niveles por periodo. Es decir,  $f(t)$  es una función periódica de periodo  $T$  y definida en el intervalo  $[0, T)$  como,

$$f(t) = \sin\left(\frac{k\pi}{8}\right) \quad \frac{kT}{16} < t < \frac{(k+1)T}{16} \quad (10)$$
$$k = 0, 1, \dots, 15$$

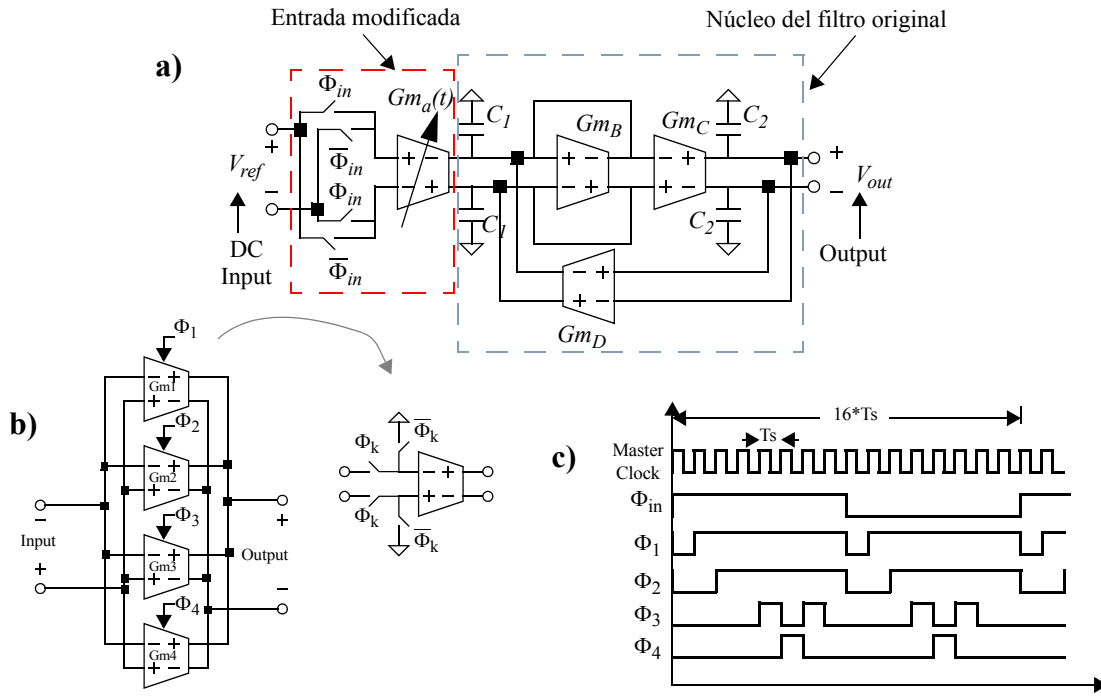
Nótese que la simetría de la función hace que sólo sean necesarios cinco valores diferentes para describir la función completa ( $k=0, 1, 2, 3, 4$ ). La elección de este tipo de función y de los filtros de segundo orden ha sido motivada por los buenos resultados que predice el análisis de Monte Carlo, junto con la simplicidad de los recursos necesarios.

En lo que sigue, los casos OTA-C y SC serán considerados de forma separada.

#### 1.3.1. Generador OTA-C

El generador desarrollado está basado en un filtro OTA-C paso de baja de segundo orden [54], [55], [57]. La Figura 9 muestra el diagrama de bloques del sistema. Para implementar el generador, los elementos de entrada del filtro se han sustituido por un esquema de conmutación controlado por la señal  $\phi_{\text{in}}$  y un transconductor programable  $G_{ma}(t)$  que recorre los valores de la senoide escalonada  $f(t)$ . El transconductor  $G_{ma}(t)$  está compuesto por cuatro transconductores en paralelo ( $G_{m1}$  a  $G_{m4}$ ) como se representa en la Figura 9b, cuyas contribuciones pueden conectarse o desconectarse de una forma incremental de acuerdo con el diagrama temporal mostrado en la Figura 9c. De esta forma se generan los cinco pasos necesarios para definir la mitad positiva de la senoide escalonada, mientras que el esquema de conmutación a la entrada controlado por  $\phi_{\text{in}}$  determina el peso (positivo o negativo) de cada escalón. La trasconductancia resultante  $G_{ma}(t)$  queda descrita por la expresión,

**FIGURA 9. a) Diagrama de bloques del generador de señal; b) Transconductor programable; c) Señales de control**



$$G_{ma}(t) = \{ \Phi_{in}(t) - \overline{\Phi_{in}(t)} \} \left\{ \sum_{k=0}^4 \Phi_k(t) G_{mk} \right\}, \quad (11)$$

donde  $G_{m0} = 0$ , y,

$$G_{mk} = G_{mA} \left[ \sin\left(\frac{k\pi}{8}\right) - \sin\left(\frac{(k-1)\pi}{8}\right) \right] \quad k = 1, 2, 3 \quad (12)$$

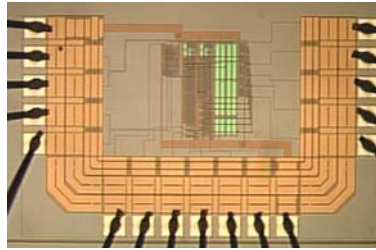
$$G_{m4} = G_{mA} \left[ \sin\left(\frac{4\pi}{8}\right) - \sin\left(\frac{2\pi}{8}\right) \right]$$

La Tabla 1 muestra el resto de parámetros de diseño para un factor de calidad  $Q$  cercano a 5, un pico de ganancia de 14dB y una frecuencia de corte sintonizable en el intervalo de 20MHz a 40MHz.

**TABLA 1. Parámetros de diseño para la Figura 9 (rango de sintonizado de la frecuencia central del filtro de 20MHz a 40MHz)**

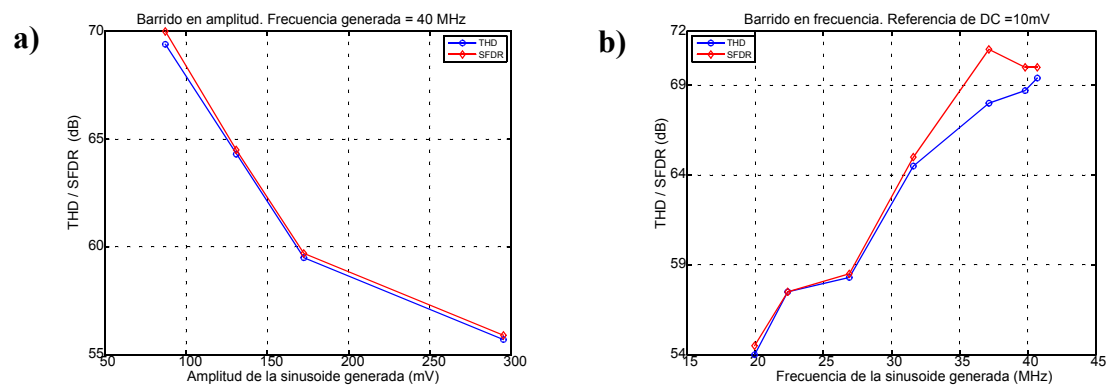
$G_{mA}$	de 275 $\mu A/V$ a 550 $\mu A/V$	$G_{mD}$	de 275 $\mu A/V$ a 550 $\mu A/V$
$G_{mB}$	de 55 $\mu A/V$ a 110 $\mu A/V$	$C_1$	4 pF
$G_{mC}$	de 275 $\mu A/V$ a 550 $\mu A/V$	$C_2$	4 pF

**FIGURA 10. Microfotografía del prototipo integrado OTA-C**



La Figura 10 muestra una microfotografía del prototipo integrado OTA-C. El sistema ocupa un área de 395 $\mu m$  por 230 $\mu m$ , excluyendo los pads. En el momento de escribir el presente documento, la falta de equipamiento adecuado hace imposible la caracterización directa del generador OTA-C en el laboratorio. Los resultados que se presentan en esta sección corresponden a simulaciones eléctricas obtenidas a partir de la vista extraída del prototipo, usando el simulador Spectre.

**FIGURA 11. THD y SFDR de la señal generada: a) en función de la amplitud de la salida; b) en función de la frecuencia de la salida**



La Figura 11 muestra la calidad de la señal generada en términos de THD y SFDR, obtenida mediante simulación eléctrica, cuando se barre tanto la amplitud como la frecuencia de la señal generada. Como se muestra en la Figura 11 la calidad de la señal disminuye con la amplitud debido al limitado rango lineal inherente a los filtros OTA-C, mientras que aumenta con la frecuencia debido a que el incremento de la corriente de alimentación necesario para mover el pico de ganancia a frecuencias más altas.

### 1.3.2. Generador SC

Para la implementación del generador SC se ha partido del biquad de Fleischer-Laker [55] como base para implementar un filtro paso de baja de segundo orden. La Figura 12 muestra el diagrama de bloques del sistema. Para implementar el generador SC, los condensadores de entrada al filtro se han sustituido por un array de cuatro condensadores ( $C_{j1}$  a  $C_{j4}$ ) que se conectan en paralelo y a los caminos de entrada de señal secuencialmente, de acuerdo al diagrama temporal mostrado en la Figura 12c. Análogamente al generador OTA-C, estos elementos de entrada programable generan los cinco pasos necesarios para definir la mitad positiva de la sinusoide escalonada, mientras que el esquema de conmutación a la entrada controlado por  $\phi_{in}$  determina el peso (positivo o negativo) de cada escalón. De esta forma, el valor de la capacidad de entrada,  $C_j(t)$ , se puede escribir como,

$$C_j(t) = \{\Phi_{in}(t) - \overline{\Phi_{in}(t)}\} \left\{ \sum_{k=0}^4 c_k(t) C_{jk} \right\} \quad (13)$$

donde,

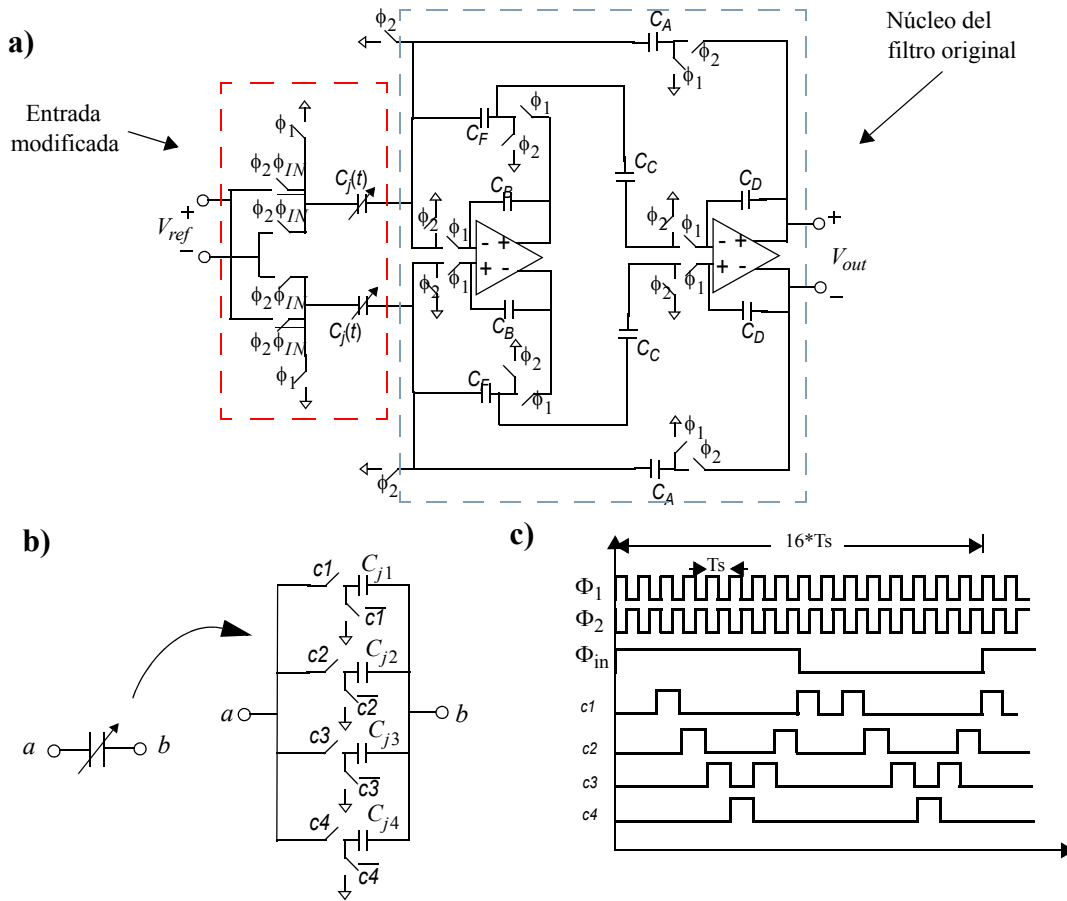
$$C_{jk} = C_J \sin \frac{k\pi}{8} \quad k = 0, 1, \dots, 4 \quad (14)$$

La Tabla 2 recoge los valores del resto de parámetros de diseño para un factor de calidad cercano a 5, un pico de ganancia de 6dB y una frecuencia de corte de un dieciseisavo de la frecuencia de reloj del filtro.

**TABLA 2. Valores de capacidad normalizados para el filtro SC de la Figura 12**

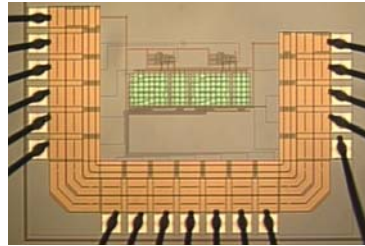
$C_A$	5.194	$C_D$	2.574
$C_B$	12.749	$C_F$	1.014
$C_C$	1	$C_J$	2

**FIGURA 12. a) Esquemático del generador de señal; b) Condensador programable; c) Relojes y señales de control**





**FIGURA 13. Microfotografía del prototipo integrado SC**

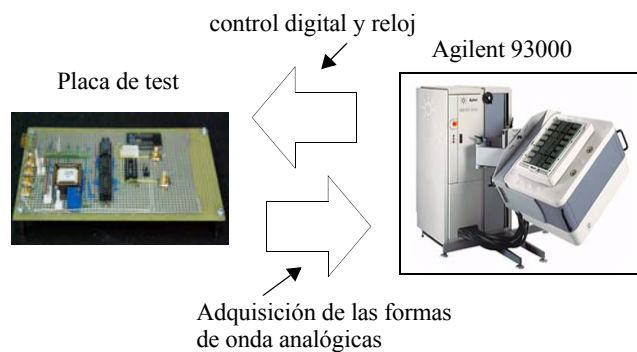


La Figura 13 muestra una microfotografía del prototipo integrado SC. El sistema ocupa un área de  $280\mu\text{m}$  por  $550\mu\text{m}$ , excluyendo los pads.

El prototipo del generador SC ha sido caracterizado en el laboratorio utilizando para ello el sistema de test de señal mixta Agilent 93000. Se han desarrollado un conjunto de experimentos destinados a probar la funcionalidad del generador y determinar la pureza espectral de las señales generadas. El montaje de test utilizado se ha representado en la Figura 14. El Agilent 93000 se ha empleado para generar las señales digitales de control y reloj, proporcionar las alimentaciones y tensiones de referencia analógicas y además adquirir y procesar la salida del generador bajo test.

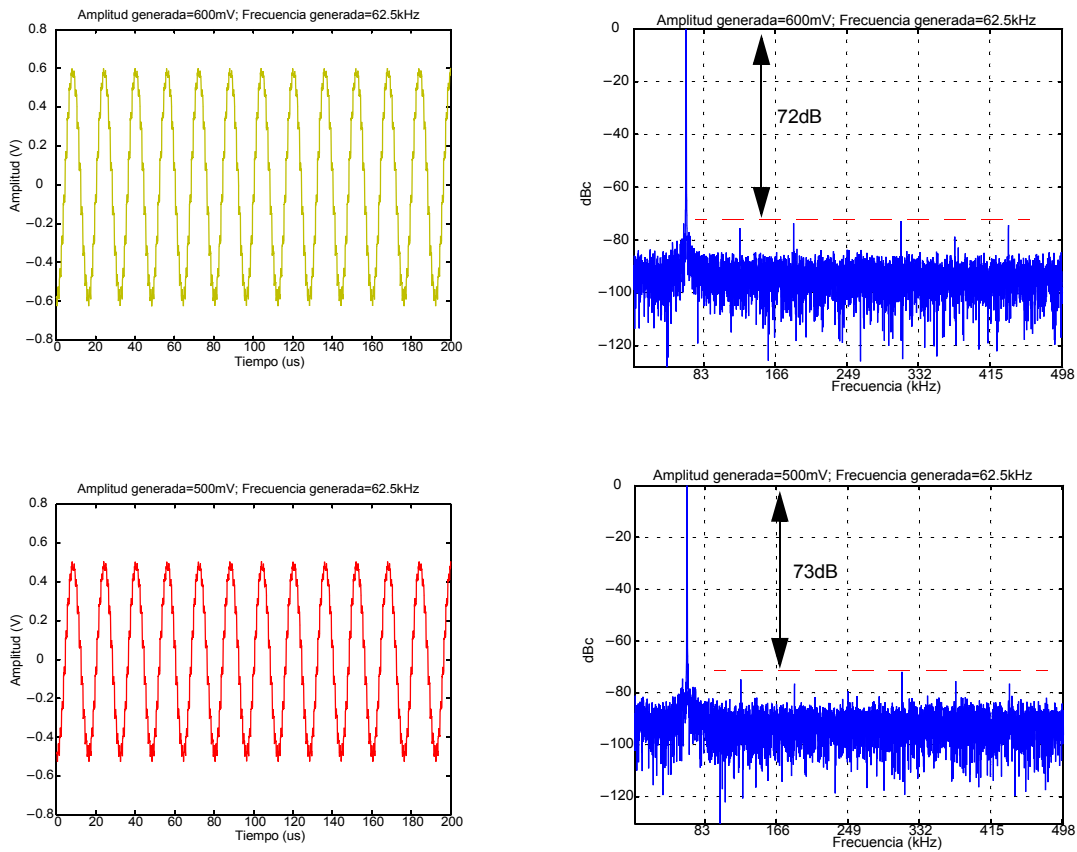
La Figura 15 muestra cuatro formas de onda generadas por el prototipo de generador junto con su espectro. La frecuencia de la señal es de  $62.5\text{kHz}$ , que se corresponde con una frecuencia de reloj de  $1\text{MHz}$ . Sus amplitudes son  $300\text{mV}$ ,  $400\text{mV}$ ,  $500\text{mV}$  y  $600\text{mV}$ , que se corresponden a los niveles de tensión de referencia a la entrada de  $150\text{mV}$ ,  $200\text{mV}$ ,  $250\text{mV}$  y  $300\text{mV}$ , respectivamente. La Figura 16 muestra las figuras de THD y SFDR obtenidas cuando se barre tanto la amplitud como la frecuencia de la señal generada.

**FIGURA 14. Esquema del montaje general de test**

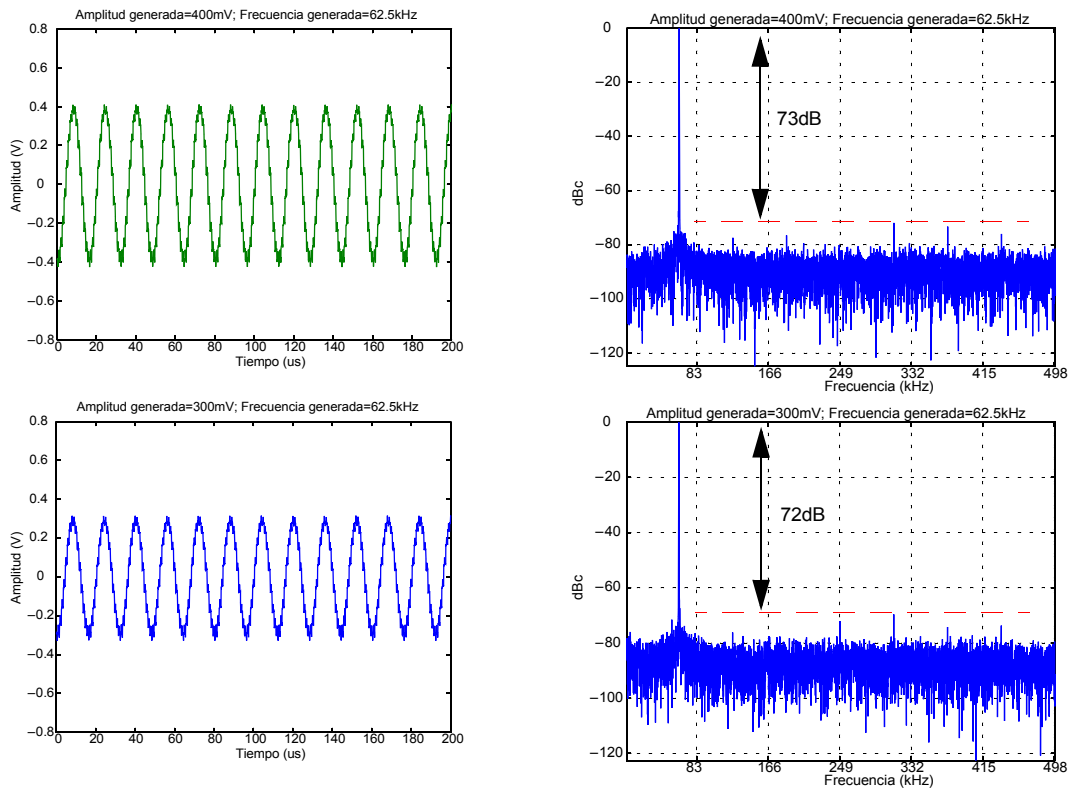


Como se desprende de los resultados presentados, las medidas de THD y SFDR son poco sensibles a los cambios de la señal generada, manteniéndose estas figuras siempre en un entorno próximo a 70dB. En realidad, este hecho es consecuencia de las limitaciones del equipo de test empleado. La placa capturadora montada en el Agilent 93000 está basada en un convertidor A/D de 12 bits que presenta figuras de linealidad muy próximas a los resultados obtenidos, lo que es indicador de que las medidas están en efecto limitadas por las prestaciones de dicho convertidor.

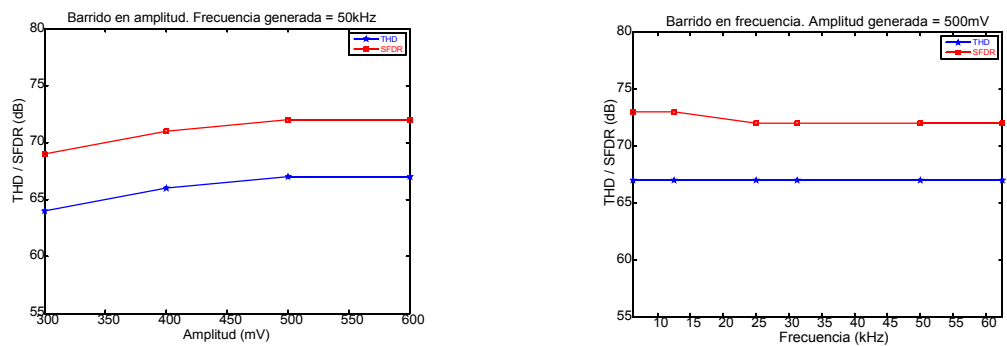
**FIGURA 15. Formas de onda generadas**



**FIGURA 15. (cont.) Formas de onda generadas**



**FIGURA 16. THD y SFDR a la salida como función de la amplitud (a) y la frecuencia (b) de la señal generada**



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## 2. Caracterización de señales analógicas periódicas para aplicaciones BIST

La caracterización de señales analógicas periódicas es uno de los puntos clave en muchos esquemas para el test de circuitos integrados analógicos y de señal mixta. La medida de parámetros tales como la respuesta en frecuencia, especificaciones de linealidad, etc., puede hacerse mediante la aplicación de un estímulo periódico y el procesado de la respuesta del sistema a dicho estímulo. Además, éste es también un punto clave en el test basado en oscilación (OBT) [71]. Este método de test consiste en convertir el DUT en un oscilador mediante una reconfiguración del mismo, de tal forma que los parámetros de la oscilación resultante (amplitud, frecuencia, nivel de DC, etc.) están directamente relacionados con las prestaciones del circuito en su operación normal [72]-[75].

### 2.1. Revisión de técnicas anteriores

Una aproximación clásica para la caracterización de señales periódicas on-chip consiste en adaptar la funcionalidad de los analizadores de espectro analógicos al marco de aplicaciones BIST. Así los trabajos en [52], [70], [76] proponen diferentes arquitecturas para la implementación on-chip de estos dispositivos. En estas aproximaciones el procesado de la señal se realiza principalmente en el plano analógico. No obstante, en muchos trabajos se prefiere trasladar el procesado al plano digital para aprovechar las características de robustez y reusabilidad propias de los circuitos digitales. En estos esquemas de caracterización hay dos puntos clave: el algoritmo de procesado digital empleado y la inevitable conversión A/D de la señal analógica que se quiere caracterizar.

Una solución común en esta línea de caracterización digital de señales analógicas periódicas consiste en el empleo de la transformada de Fourier, implementada normalmente como un algoritmo FFT (Fast Fourier Transform) tras una conversión de la señal al dominio digital. Sin embargo, la implementación directa de este esquema no suele ser práctica debido a su excesivo coste a no ser que el hardware requerido se encuentre en el sistema y pueda ser reutilizado en la fase de test. Así, existen múltiples trabajos que proponen algoritmos digitales optimizados como alternativa al cálculo directo de la FFT [79], [80], [81].

Una desventaja de los algoritmos digitales de procesado es que, en general, requieren el empleo de un convertidor A/D completo como interfaz entre la señal analógica y el bloque de procesado. Convertidor que, en última instancia, va a limitar las prestaciones del sistema y que además puede ser difícil de implementar para aplicaciones de alta precisión. En este sentido, se han presentado muchos trabajos centrados en simplificar el interfaz A/D necesario en el esquema de caracterización. Una técnica que se ha demostrado muy eficiente para la evaluación on-chip de señales analógicas es la codificación  $\Sigma\Delta$  [85]-[87].

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## 2.2. Estrategia propuesta para la caracterización de señales periódicas

Esta sección presenta un novedoso método para la caracterización on-chip de señales analógicas periódicas basado en una aproximación de la serie trigonométrica de Fourier. La técnica de análisis propuesta permite la extracción de los parámetros característicos de una señal periódica, esto es, su nivel de DC, y la amplitud y fase de sus componentes armónicas.

Como se ha apuntado anteriormente, un sistema eficiente para la caracterización de señales analógicas en el plano digital tienen que tener en cuenta dos factores: la interfaz de conversión A/D y el algoritmo de procesamiento digital. Ambos puntos se tratarán en detalle en las siguientes secciones. Primeramente se va a analizar el algoritmo propuesto y a continuación nos centraremos en la implementación de un interfaz A/D eficiente adaptado a dicho algoritmo.

### 2.2.1. Base teórica: algoritmo de procesamiento

Consideremos una señal  $x(t)$  periódica definida en el intervalo  $[0, T)$  y de cuadrado integrable en dicho intervalo. El procedimiento estándar para caracterizar este tipo de señales consiste en desarrollar la señal en su serie de Fourier para extraer sus componentes armónicas, en la forma [88],

$$x(t) = a_0 + \sum_{k=1}^{\infty} [a_k \cos(k\omega t) + b_k \sin(k\omega t)] \quad (15)$$

donde  $\omega=2\pi/T$ , y los coeficientes  $a_0$ ,  $a_k$ , y  $b_k$ , para todo  $k$  entero y positivo, están definidos por,

$$a_0 = \frac{1}{T} \int_0^T x(t) dt \quad (16)$$

$$a_k = \frac{2}{T} \int_0^T x(t) \cos(k\omega t) dt \quad (17)$$

$$b_k = \frac{2}{T} \int_0^T x(t) \sin(k\omega t) dt \quad (18)$$

Así, la señal  $x(t)$  está completamente caracterizada por el conjunto de coeficientes de su desarrollo en serie de Fourier  $\{a_0, a_k, b_k\}$ . La ecuación (15) se puede reescribir como,

$$x(t) = B + \sum_{k=1}^{\infty} A_k \sin(k\omega t + \varphi_k) \quad (19)$$

donde  $B$  representa un nivel de DC,  $A_k$  es la amplitud de la componente armónica  $k$ -ésima y  $\varphi_k$  es su correspondiente fase. Los coeficientes  $\{B, A_k, \varphi_k\}$  están relacionados con el conjunto de parámetros  $\{a_0, a_k, b_k\}$  mediante las expresiones,

$$\begin{aligned} a_0 &= B \\ a_k &= A_k \sin \varphi_k \\ b_k &= A_k \cos \varphi_k \end{aligned} \quad (20)$$

Es claro que los coeficientes  $\{B, A_k, \varphi_k\}$  también caracterizan completamente a la señal  $x(t)$ . Sin embargo, el cálculo de ambos conjuntos de coeficientes,  $\{a_0, a_k, b_k\}$  o  $\{B, A_k, \varphi_k\}$ , implica el cálculo de (16)-(18). Es decir, la señal debe ser modulada por las autofunciones seno y coseno, e integrada de manera continua en el tiempo. Ambas operaciones son demasiado costosas para su inclusión on-chip. En lugar de eso, vamos a proponer una aproximación de (16)-(18) que, como será demostrado, nos ayudará a definir un nuevo algoritmo para la caracterización de señales periódicas muy adecuado para su implementación on-chip. Nuestra propuesta consta de dos puntos principales: la sustitución de las autofunciones seno y coseno por dos ondas cuadradas en cuadratura, y la discretización de la señal. Por simplicidad, vamos a considerar ahora de forma aislada el efecto del primero de estos puntos, mientras que la discretización de la señal se estudiará en la siguiente sección junto con la introducción del interfaz A/D.

Sean las señales  $SQ_k^T(t)$  y  $SQ_k^T\left(t - \frac{T}{4k}\right)$  dos ondas cuadradas en cuadratura, de periodo  $T/k$  y amplitud unidad. Con estas señales definimos dos firmas  $\hat{I}_{1k}$  e  $\hat{I}_{2k}$  como,

$$\begin{aligned} \hat{I}_{1k} &= \frac{1}{T} \int_0^T x(t) SQ_k^T(t) dt & k = 0, 1, 2, \dots \\ \hat{I}_{2k} &= \frac{1}{T} \int_0^T x(t) SQ_k^T\left(t - \frac{T}{4k}\right) dt & k = 0, 1, 2, \dots \end{aligned} \quad (21)$$

Es decir,  $\hat{I}_{1k}$  e  $\hat{I}_{2k}$  son la integración continua de la señal  $x(t)$  modulada por dos ondas cuadradas en cuadratura, sobre un periodo completo de la señal. Sustituyendo el desarrollo en (19) en la

definición de las firmas (21) se puede determinar la contribución de cada término del desarrollo a las firmas,

$$I_{10} = I_{20} = B$$

$$\hat{I}_{1k} = \frac{2}{\pi} \left( A_k \cos \varphi_k + \sum_{i=1}^{\infty} \frac{A_{(2i+1)k}}{(2i+1)} \cos \varphi_{(2i+1)k} \right) \quad k = 1, 2, \dots \quad (22)$$

$$\hat{I}_{2k} = \frac{2}{\pi} \left( A_k \sin \varphi_k + \sum_{i=1}^{\infty} \frac{A_{(2i+1)k}}{(2i+1)} \sin \varphi_{(2i+1)k} \right) \quad k = 1, 2, \dots$$

donde se ha considerado que  $SQ_k^T(t) = SQ_k^T\left(t - \frac{T}{4k}\right) = 1$  en el caso  $k=0$  y que las fases  $\varphi_k$  están referidas al flanco positivo de  $SQ_k^T(t)$ .

Si restringimos la discusión a señales limitadas en banda, es decir, con un número finito de componentes armónicas significativas, que es el caso usual en aplicaciones de test, es posible simplificar la expresión (22). Por ejemplo, si consideramos que  $x(t)$  sólo tiene cuatro componentes armónicas significativas, que es un caso típico en aplicaciones de test, la Tabla 3 muestra los resultados de las firmas para los diferentes valores de  $k$ . De los valores de las firmas que se recogen en Tabla 3 es directo determinar los parámetros característicos de la señal  $x(t)$ ,

$$B = \hat{I}_{10} = \hat{I}_{20} \quad (23)$$

$$A_k^2 = \left(\frac{\pi}{2}\right)^2 [(\hat{I}_{1k})^2 + (\hat{I}_{2k})^2] \quad k = 1, \dots, 4 \quad (24)$$

$$\tan \varphi_k = \frac{\hat{I}_{2k}}{\hat{I}_{1k}} \quad k = 1, \dots, 4 \quad (25)$$

**TABLA 3. Firmas  $\hat{I}_{1k}$  e  $\hat{I}_{2k}$  para diferentes valores de  $k$  y cuatro componentes armónicas significativas**

$k$	$\hat{I}_{1k}$	$\hat{I}_{2k}$
0	$B$	$B$
1	$\frac{2}{\pi} \left[ A_1 \cos \varphi_1 + \frac{A_3}{3} \cos \varphi_3 \right]$	$\frac{2}{\pi} \left[ A_1 \sin \varphi_1 + \frac{A_3}{3} \sin \varphi_3 \right]$
2	$\frac{2}{\pi} A_2 \cos \varphi_2$	$\frac{2}{\pi} A_2 \sin \varphi_2$
3	$\frac{2}{\pi} A_3 \cos \varphi_3$	$\frac{2}{\pi} A_3 \sin \varphi_3$
4	$\frac{2}{\pi} A_4 \cos \varphi_4$	$\frac{2}{\pi} A_4 \sin \varphi_4$

donde se ha considerado que  $A_1 \gg \frac{A_3}{3}$ . En cualquier caso, si la aproximación anterior no se verifica, es fácil eliminar la contribución de  $A_3$  y  $\varphi_3$  en las firmas para  $k=1$ , dado que ambos se calculan aisladamente para  $k=3$ .

### 2.2.2. Interfaz A/D: modulador $\Sigma\Delta$ de primer orden y tiempo discreto

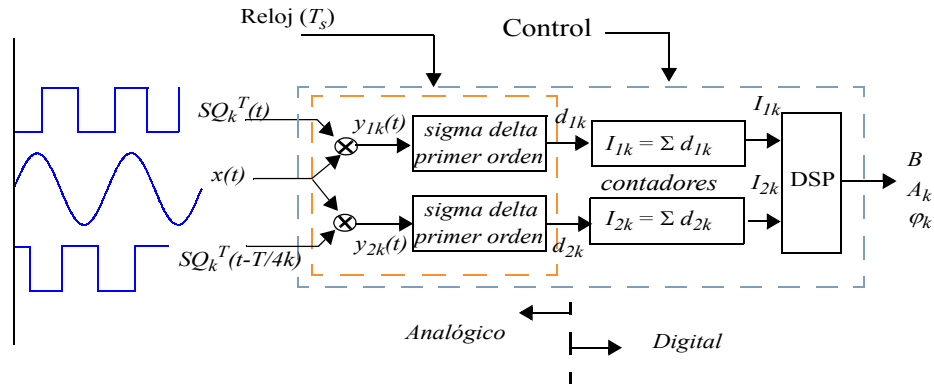
Los resultados matemáticos obtenidos en la sección anterior se pueden utilizar para construir un sistema eficiente para la caracterización de señales periódicas analógicas en base a las firmas  $\hat{I}_{1k}$  e  $\hat{I}_{2k}$ . Los recursos necesarios para el cálculo de las firmas de una determinada señal se reducen a la integración de dicha señal modulada por dos ondas cuadradas en cuadratura.

Realizar la integración en el dominio analógico no suele ser práctico. Es claramente más ventajoso realizar esta operación en el plano digital tras una discretización y conversión de la señal al plano digital. Sin embargo, como se ha comentado anteriormente, la inclusión de un convertidor A/D completo puede ser problemático para una implementación BIST. La implementación que proponemos usa una modulación  $\Sigma\Delta$  de primer orden con un cuantizador de un bit en vez de una conversión A/D completa para llevar a cabo la conversión de una forma simple y robusta, a la vez que se aprovechan las propiedades de conformación de ruido propias de la modulación  $\Sigma\Delta$  para obtener una buena precisión en las medidas.

La Figura 17 muestra el diagrama de bloques de la implementación propuesta. La señal que se pretende caracterizar,  $x(t)$ , es modulada por dos ondas cuadradas en cuadratura,  $SQ_n^T(t)$  y



FIGURA 17. Esquema propuesto para la implementación del analizador de señal



$SQ_n^T\left(t - \frac{T}{4n}\right)$ . Las señales resultantes,  $y_{1k}(t)$  e  $y_{2k}(t)$ , entran a dos moduladores  $\Sigma\Delta$  de primer orden. Las cadenas de bits que generan los moduladores,  $d_{1k}(n)$  e  $d_{2k}(n)$  son integradas sobre un número  $M$  de periodos de señal usando sendos contadores para obtener las firmas  $I_{1k}$  e  $I_{2k}$  definidas como,

$$I_{1k} = \sum_{n=1}^{MN} d_{1k}(n) \quad (26)$$

$$I_{2k} = \sum_{n=1}^{MN} d_{2k}(n)$$

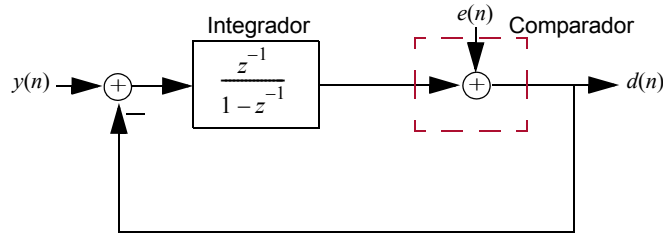
Finalmente un procesamiento digital permite obtener las medidas de los parámetros de la señal de entrada a partir de las firmas.

Para analizar el esquema de la Figura 17 en términos de precisión en las medidas vamos a considerar el modelo lineal para un modulador  $\Sigma\Delta$  de primer orden que se muestra en la Figura 18. En adelante, el *full scale* del modulador se considerará unidad (las magnitudes serán entonces normalizadas al *full scale*), y la razón de sobremuestreo  $N$  será un múltiplo de  $2^3k$ , de tal forma que tanto  $N$  como  $N/4k$  son números enteros.

La respuesta  $d(n)$  a la salida del modulador de la Figura 18 se puede expresar como una función de la entrada  $y(n)$  y del error de cuantización  $e(n)$  como,

$$d(n) = y(n-1) + \{e(n) - e(n-1)\} \quad (27)$$

**FIGURA 18. Modelo lineal de un modulador  $\Sigma\Delta$  de primer orden**



donde  $y(n)=y(nT_s)$  y  $T_s$  es el periodo de muestreo.

La integración discreta de la cadena de bits sobre  $P$  muestras a la salida del modulador será,

$$\sum_{n=1}^P d(n) = \sum_{n=0}^{P-1} y(n) + \{e(P) - e(0)\} \quad (28)$$

Asumiendo que no se sobrepasa en ningún momento el *full scale* del modulador, el error  $e(n)$  pertenece al intervalo  $[-1, 1]$ , de forma que el error de cuantización introduce un error en la integración discreta de  $\pm 2$ . Si la integración discreta se extiende a un número entero de periodos  $M$ , entonces el número total de muestras integradas será  $P=MN$ , mientras que el término de error  $\pm 2$  permanece constante. Esto significa que el error relativo de las medidas disminuye en un factor  $M$  con respecto a la integración sobre un solo periodo de señal.

Además, si la razón de sobremuestreo es suficientemente alta, la integración discreta de  $y(n)$  tiende a la integración continua de  $y(t)$ , dado que el error cometido es despreciable respecto al error de cuantización. En el caso de que esta aproximación no sea válida, hay que tener en cuenta en el cálculo el efecto del muestreo: la medida aparece entonces modulada por una función *sampling*. La Tabla 4 muestra las firmas  $I_{1k}$  e  $I_{2k}$  a la salida de los contadores para cada componente armónica  $k$  como función de la razón de sobremuestreo  $N$ , y del número de periodos de integración  $M$  (por simplicidad se ha supuesto que  $x(t)$  tiene sólo cuatro componentes armónicas significativas y que  $N$  es suficientemente grande). Nótese además que las firmas  $I_{1k}$  e  $I_{2k}$ , debido a su definición, son siempre números enteros comprendidos entre los valores extremos definidos por el error de cuantización.

**TABLA 4. Valores de las firmas  $I_{1k}$  e  $I_{2k}$  para diferentes valores de  $k$  y cuatro componentes armónicas significativas**

$k$	$I_{1k}$	$I_{2k}$
0	$MNB \pm 2$	$MNB \pm 2$
1	$\frac{2MN}{\pi} \left( A_1 \cos \varphi_1 + \frac{A_3}{3} \cos \varphi_3 \right) \pm 2$	$\frac{2MN}{\pi} \left( A_1 \sin \varphi_1 + \frac{A_3}{3} \sin \varphi_3 \right) \pm 2$
2	$\frac{2MN}{\pi} A_2 \cos \varphi_2 \pm 2$	$\frac{2MN}{\pi} A_2 \sin \varphi_2 \pm 2$
3	$\frac{2MN}{\pi} A_3 \cos \varphi_3 \pm 2$	$\frac{2MN}{\pi} A_3 \sin \varphi_3 \pm 2$
4	$\frac{2MN}{\pi} A_4 \cos \varphi_4 \pm 2$	$\frac{2MN}{\pi} A_4 \sin \varphi_4 \pm 2$

Los parámetros característicos de la señal bajo estudio  $x(t)$ , es decir, su nivel de DC y las amplitudes y fases de sus componentes armónicas, se pueden estimar a partir de las firmas. De esta forma, se puede asegurar que,

$$B \in \frac{1}{MN} [\min(I_{10} + \varepsilon_{10}), \max(I_{10} + \varepsilon_{10})] \quad \text{ó} \quad (29)$$

$$\frac{1}{MN} [\min(I_{20} + \varepsilon_{20}), \max(I_{20} + \varepsilon_{20})]$$

$$(A_k)^2 \in \left( \frac{\pi}{2MN} \right)^2 \left[ \begin{array}{l} \min \{ (I_{1k} + \varepsilon_{1k})^2 + (I_{2k} + \varepsilon_{2k})^2 \}, \\ \max \{ (I_{1k} + \varepsilon_{1k})^2 + (I_{2k} + \varepsilon_{2k})^2 \} \end{array} \right] \quad (30)$$

$$\tan \varphi_k \in \left[ \min \left( \frac{I_{2k} + \varepsilon_{2k}}{I_{1k} + \varepsilon_{1k}} \right), \max \left( \frac{I_{2k} + \varepsilon_{2k}}{I_{1k} + \varepsilon_{1k}} \right) \right] \quad (31)$$

donde los términos  $\varepsilon_{1k}$ ,  $\varepsilon_{2k}$  ( $k=0, 1, 2, \dots$ ) son términos de error debidos al error de cuantización y limitados a  $\varepsilon_{1k}, \varepsilon_{2k} \in [-2, 2]$ . Nótese que se ha asumido que  $\frac{2MNA_3}{3\pi} < 1$ . Si esto no fuera así, sería necesario tener en cuenta la contribución de  $A_3$  en el cálculo de  $A_1$ , dado que ésta se calcula de forma aislada para  $k=3$ .

Hasta este momento no se ha considerado el efecto del offset del modulador sobre las medidas. No obstante, si el modulador presenta un offset  $V_{off}$ , las firmas  $I_{1k}$  e  $I_{2k}$  serán corrompidas en un factor  $MNV_{off}$ , dado que este offset se integra junto con las señales moduladas. Si  $MNV_{off} > 1$ , entonces es necesario compensar este efecto para mantener la precisión de las medidas. Una estrategia sencilla para conseguir esta compensación consiste en cambiar el signo de la modulación cuadrada a la mitad del tiempo de evaluación. El número total de periodos de evaluación debe ser par en este caso. Se obtienen entonces un par de firmas  $I_\alpha$  e  $I_\beta$  para cada una de las firmas originales  $I_{1k}$  e  $I_{2k}$ , donde  $I_\alpha$  corresponde a la integración sobre la primera mitad de la evaluación, e  $I_\beta$  corresponde a la segunda mitad. Dado que el offset no es modulado, puede compensarse restando ambas firmas parciales. Este método tiene la contrapartida de que los errores de cuantización de las firmas parciales se suman al realizar la sustracción, por lo que el error en la medida se hace doble. Para mantener la misma precisión es necesario duplicar el número de periodos de evaluación.

También es importante hacer notar que la técnica de medida presentada necesita sincronización entre la señal a caracterizar y el reloj de muestreo, de forma que la razón de sobremuestreo  $N$  sea un múltiplo de  $2^3k$ , y tanto  $N$  como  $N/4k$  sean números enteros. Esta sincronización se puede conseguir de diversas maneras. Por ejemplo, si el estímulo de test viene dado por un generador de señal controlado por un reloj maestro (como sería el caso de ATEs externos, o bien de generadores on-chip como el presentado en este mismo trabajo en la sección anterior), entonces basta usar el mismo reloj para generar la señal de test y las correspondientes señales de control para conseguir la sincronización. En otros casos se puede usar un PLL convenientemente adaptado para esta tarea.

### 2.2.3. Validación de la implementación propuesta

La viabilidad de la implementación propuesta se ha verificado en SIMULINK/MATLAB. El diagrama de bloques del analizador mostrado en la Figura 17 se ha implementado usando un modelo de comportamiento para los moduladores  $\Sigma\Delta$  de primer orden que contempla sus principales no idealidades y usando una descripción de comportamiento para los contadores y el bloque DSP. Las condiciones de la simulación se recogen en la Tabla 5.

**TABLA 5. Condiciones de simulación**

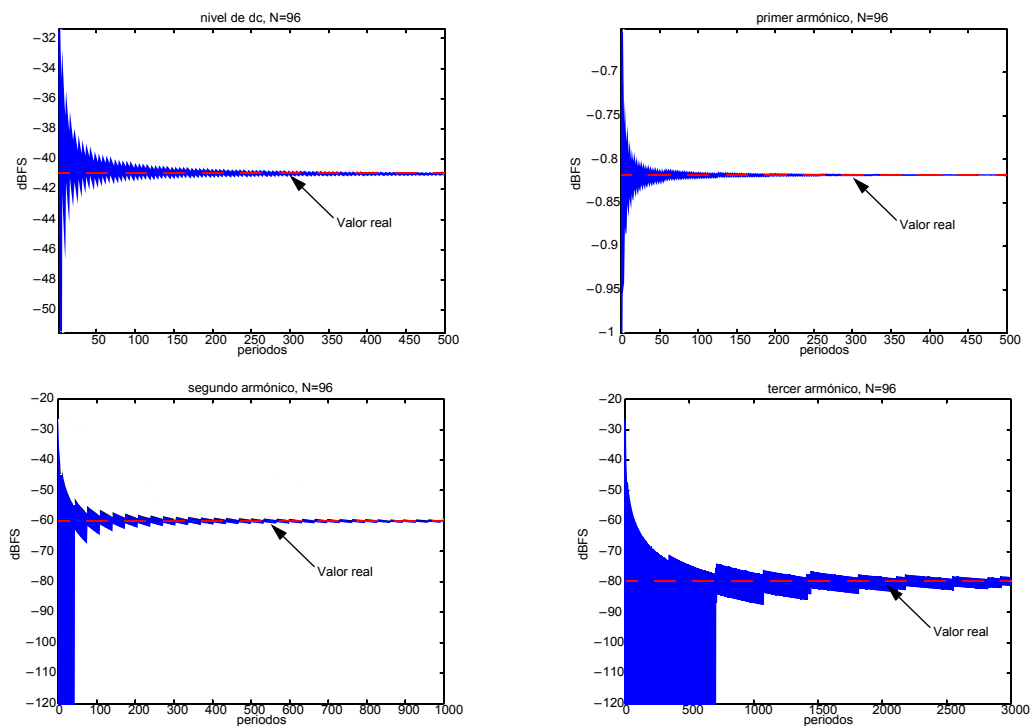
<b>Offset del modulador</b>	aleatorio (de $-10\text{mV}$ a $10\text{mV}$ )
<b>Coefficiente de pérdidas en el integrador, <math>\alpha</math></b>	0.99999
<b>Histéresis en el comparador</b>	6mV
<b>Temperatura</b>	300K
<b>Clock jitter (valor máximo)</b>	1ns
<b>Razón de sobremuestreo</b>	144

La señal de entrada usada para validar el sistema contiene tres componentes armónicas,  $A_1$ ,  $A_2$  y  $A_3$ , y un nivel de DC (véase la Tabla 6). La Figura 19 muestra la evolución del intervalo de confianza obtenido en cada medida para un sobremuestreo  $N=96$  como función del número de periodos de evaluación  $M$ . Los resultados están de acuerdo con los resultados esperados, y muestran como la precisión de las medidas para una determinada magnitud aumenta con el número de periodos de evaluación..

**TABLA 6. Componentes de la señal de entrada. Valores en dBFS normalizados respecto al full scale del modulador**

Componente	Nivel de DC	$A_1$	$A_2$	$A_3$	Fases, $\varphi_1, \varphi_2, \varphi_3$
Valor real	-41.01 dBFS	-0.82 dBFS	-60 dBFS	-80 dBFS	aleatorias

**FIGURA 19. Intervalos de confianza frente al número de periodos de evaluación**



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## 2.3. Prototipo integrado

La implementación propuesta para el analizador de señales periódicas (véase Figura 17) requiere de una doble modulación, cuadrada y  $\Sigma\Delta$ , junto con un algoritmo digital de procesamiento muy simple. En esta sección se presenta el diseño de un prototipo demostrador de la técnica de análisis propuesta.

Se ha empleado una tecnología CMOS estándar de  $0.35\mu\text{m}$  para diseñar un prototipo del sistema propuesto en la Figura 17, con el objetivo de caracterizar señales periódicas en el rango de frecuencias de audio (hasta 20kHz). Aunque sólo se ha integrado la parte analógica del sistema, en esta sección también se hacen consideraciones sobre el diseño de la parte digital.

### 2.3.1. Parte analógica: modulador $\Sigma\Delta$ de primer orden con modulación cuadrada a la entrada

La Figura 20 muestra un diagrama de bloques del modulador  $\Sigma\Delta$  de primer orden implementado. Se ha escogido una implementación SC completamente diferencial, que funciona con dos fases de reloj no solapadas  $\phi_1$  y  $\phi_2$ . La modulación cuadrada ha sido incluida a la entrada del modulador mediante un esquema de conmutación controlado por la señal  $q_k$ . Cuando la señal  $q_k$  cambia de estado, el efecto sobre la entrada es equivalente a un cambio de signo, lo que consigue la modulación cuadrada deseada.

Es importante señalar que el modulador  $\Sigma\Delta$  es el bloque que limita las prestaciones del analizador en conjunto. Las prestaciones del modulador  $\Sigma\Delta$  van a limitar el rango de señal (tanto en amplitud como en frecuencia) que es posible medir. En este sentido, existen moduladores  $\Sigma\Delta$  que trabajan en el rango de decenas de MHz [92]-[94], lo que significa que la estrategia de medida propuesta podría extenderse a señales del orden de algunos MHz manteniendo una razón de sobremuestreo razonablemente alta. Además, una implementación en tiempo continuo del modulador también es posible y permitiría extender el rango de aplicación a frecuencias más altas [95]-[96].

### 2.3.2. Parte digital: bloque de procesamiento digital de señal (DSP)

Con respecto al DSP, la evaluación de las componentes armónicas de la señal requiere dos contadores para el cálculo de las firmas  $I_{1k}$  e  $I_{2k}$ , un bloque para elevar al cuadrado las firmas y un bloque sumador para obtener la firma de cada componente  $(I_{1k})^2 + (I_{2k})^2$ . La Figura 21 muestra un diagrama de bloques simplificado del DSP.

Un punto importante en el esquema de proceso digital propuesto es la implementación de la función elevar a la cuadrado. Dado que esta función sólo se usa un número limitado de veces ( $2L$  veces para caracterizar  $L$  componentes), es ventajoso realizar esta operación secuencialmente en varios ciclos de reloj. Así, el cálculo del cuadrado de un número de  $n$  bits se puede reducir al cálculo

FIGURA 20. Modulador  $\Sigma\Delta$  de primer orden con modulación cuadrada a la entrada

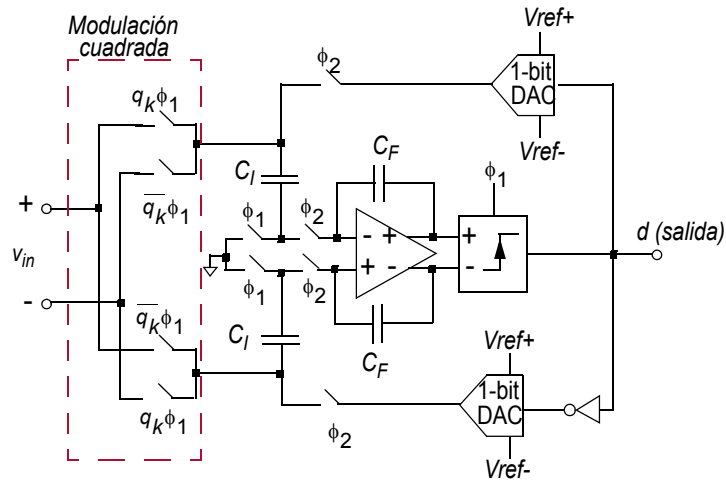
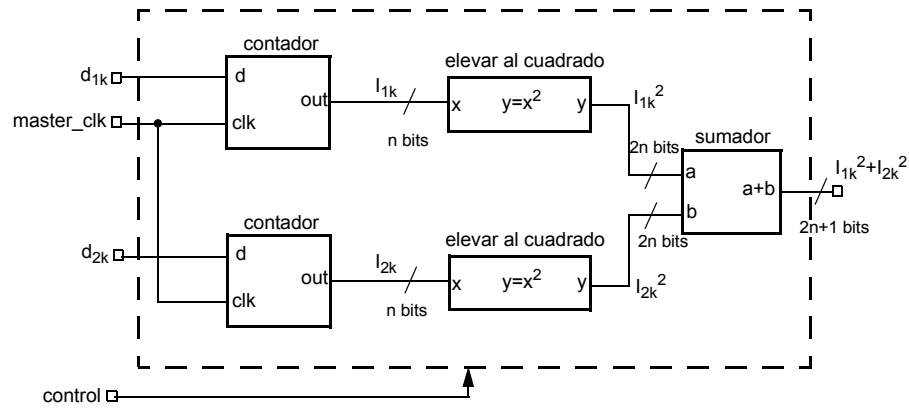
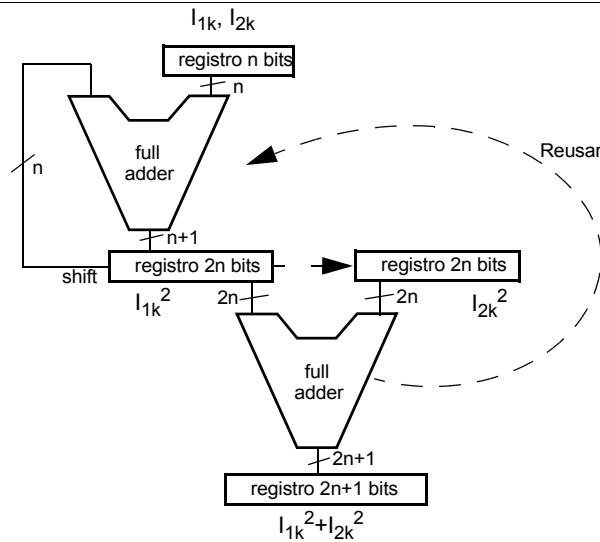


FIGURA 21. Diagrama de bloques del DSP



de  $n$  sumas que se pueden realizar en  $n$  ciclos de reloj. La Figura 22 muestra un diagrama de bloques en el que se muestra esta estrategia secuencial de procesamiento.

**FIGURA 22. Implementación secuencial para el cálculo de los cuadrados**



## 2.4. Resultados

La parte analógica del analizador se ha integrado en una tecnología CMOS estándar de  $0.35\mu\text{m}$ . La simplicidad del DSP permite su implementación vía software, lo cual permite una mayor flexibilidad en el test del prototipo del analizador. La Figura 23 muestra una microfotografía del prototipo integrado. Ocupa un área de  $0.065\text{mm}^2$ .

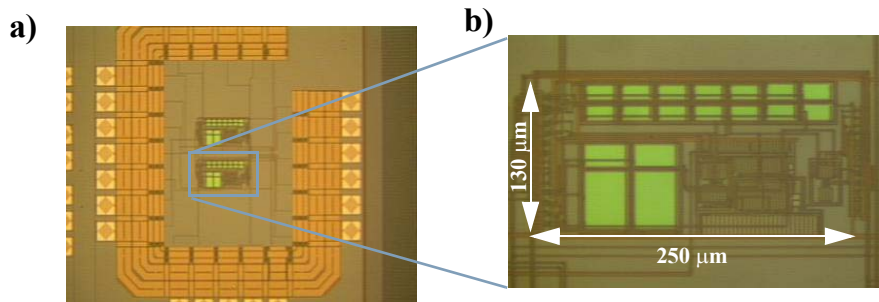
Sobre la parte digital, aunque no ha sido integrada, se puede dar una estimación de área. La Figura 24 muestra una síntesis directa del bloque DSP indicado en la sección anterior para contadores de 16 bits. Para la síntesis se ha usado la librería de celdas estándar de la misma tecnología de  $0.35\mu\text{m}$  usada en la integración de la parte analógica, y ocupa un área de  $300\mu\text{m}$  por  $300\mu\text{m}$  aproximadamente.

Sobre el prototipo integrado se han llevado a cabo diferentes experimentos para verificar que el comportamiento del analizador de señales se corresponde con el esperado teóricamente.

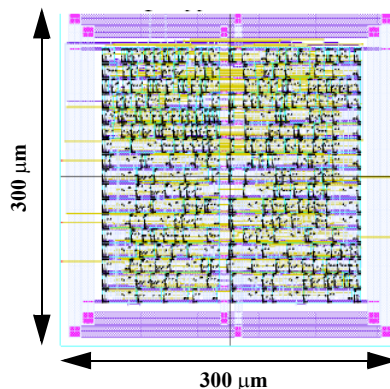
La Figura 25a representa los códigos digitales correspondientes a medidas de amplitud sobre una señal de entrada monotonal cuya amplitud se ha variado desde  $1\text{mV}$  hasta  $600\text{mV}$ . La frecuencia de muestreo se ha fijado en  $1\text{MHz}$ , lo que fija la razón de sobremuestreo en  $N=144$ , mientras que el número de periodos de evaluación se ha fijado en  $M=20$ . Los códigos obtenidos muestran un comportamiento lineal y están confinados en una banda con un error de  $\pm 3$ , lo que está en perfecto



**FIGURA 23. Microfotografías del prototipo: a) Vista general b) Detalle del modulador  $\Sigma\Delta$**



**FIGURA 24. DSP sintetizado usando celdas estándar en una tecnología de 0.35μm**

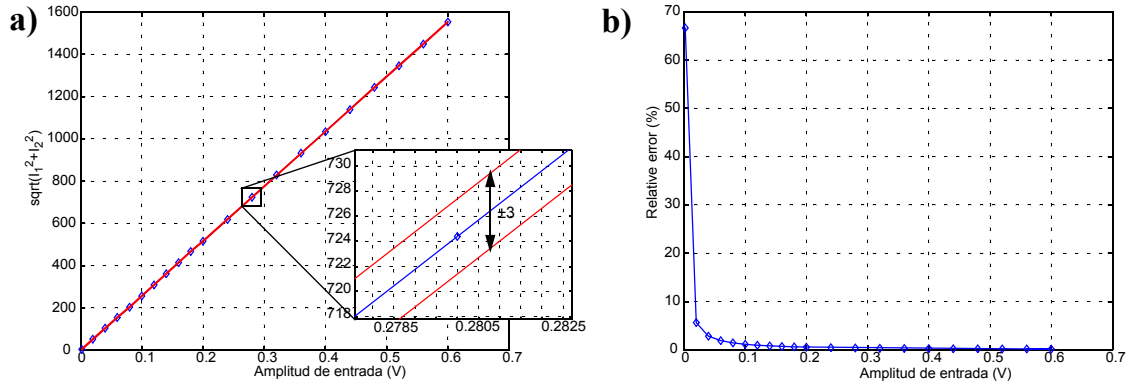


acuerdo con el máximo error esperado de  $\pm 4$  (es conveniente señalar que se ha usado un algoritmo de compensación del offset del modulador que duplica el error esperado original de  $\pm 2$ ). Los resultados obtenidos están de acuerdo con lo esperado teóricamente. La Figura 25b muestra como el error relativo de la medida disminuye con la amplitud de la señal.

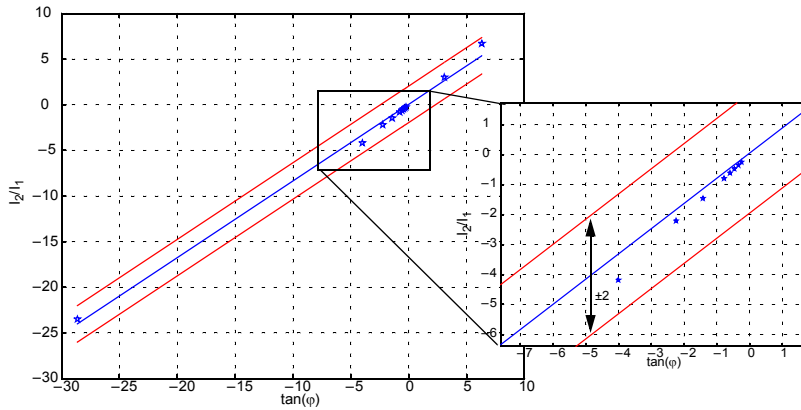
La Figura 26 muestra la capacidad del sistema para realizar medidas de fase. La señal de entrada es un tono de amplitud 400mV, cuya fase respecto a la función de modulación cuadrada  $SQ_k^T(t)$  se ha variado desde  $-10^\circ$  hasta  $-100^\circ$ . La Figura 26 muestra los correspondientes códigos digitales frente a los valores reales. El número de muestras se ha fijado a  $N=96$  y  $M=200$ . La característica lineal y la banda de error limitada a  $\pm 2$  está de acuerdo con lo esperado teóricamente.

La Figura 27 muestra medidas de la componente de offset de la señal de entrada. La entrada se ha fijado a un tono de amplitud 200mV y offset nulo. La Figura 27 muestra un histograma de las

**FIGURA 25. a) Resultados experimentales para diferentes valores de la amplitud de entrada; b) Error relativo de las medidas**

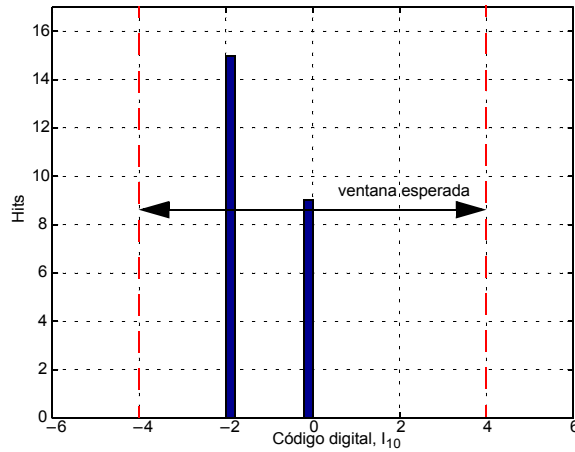


**FIGURA 26. Medidas experimentales de la fase de la señal de entrada**



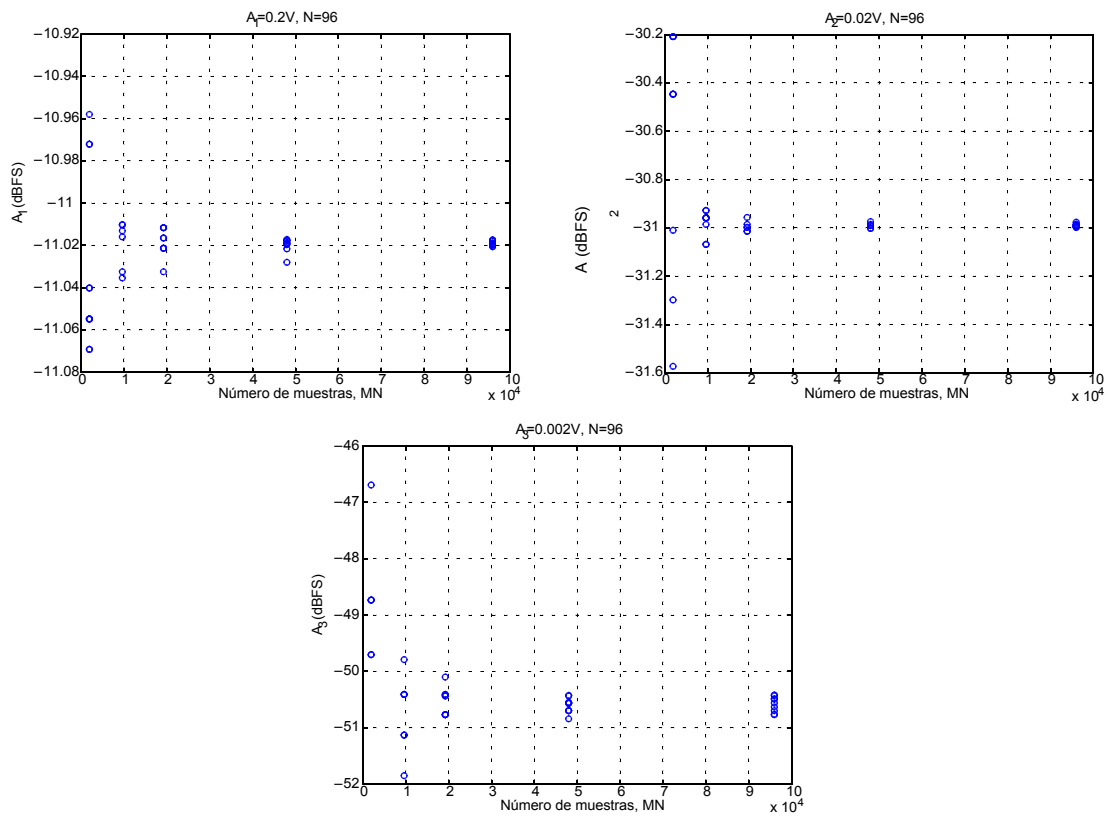
medidas de offset de esta señal cuando el número de muestras se fija a  $N=144$  y  $M=2$ . Los códigos digitales obtenidos están dentro de la ventana de valores esperados teóricamente.

FIGURA 27. Histograma de medidas de offset



Finalmente, la Figura 28 muestra las medidas relativas al *full-scale* del modulador de las componentes armónicas de una señal multitono compuesta por tres componentes:  $A_1=200\text{mV}$ ,  $A_2=20\text{mV}$ , y  $A_3=2\text{mV}$ . La razón de sobremuestreo se ha fijado en  $N=96$  y el número de periodos de evaluación se ha variado de  $M=20$  a  $M=1000$ . El experimento se ha repetido 25 veces para cada valor de  $M$ , para demostrar que las medidas son repetibles.

**FIGURA 28. Medida de componentes armónicas como función del número de muestras de evaluación. Sobremuestreo  $N=96$**



### 3. Un analizador de redes/espectros para aplicaciones BIST

Las técnicas de análisis de la respuesta en frecuencia y su adaptación a esquemas de test BIST se han convertido en los últimos años en un tema que despierta gran interés en la comunidad de test. Así, se han presentado diversas técnicas BIST para la caracterización en frecuencia de circuitos analógicos y muchas de ellas se han demostrado experimentalmente con prototipos integrados [50],[52],[70],[78],[81],[83],[99].

En esta sección vamos a combinar las técnicas de generación de sinusoides y caracterización de señales periódicas previamente presentadas para construir un sistema BIST completo capaz de caracterizar la respuesta en frecuencia de un sistema analógico en términos de magnitud, fase, distorsión armónica y medida de offset.

#### 3.1. Descripción del sistema

La Figura 29 muestra el diagrama de bloques del sistema de test propuesto. Se compone de tres bloques principales, aparte del DUT:

- El generador de señales sinusoidales basado en la técnica SC presentado anteriormente.

**FIGURA 29. Diagrama de bloques del sistema de caracterización propuesto**

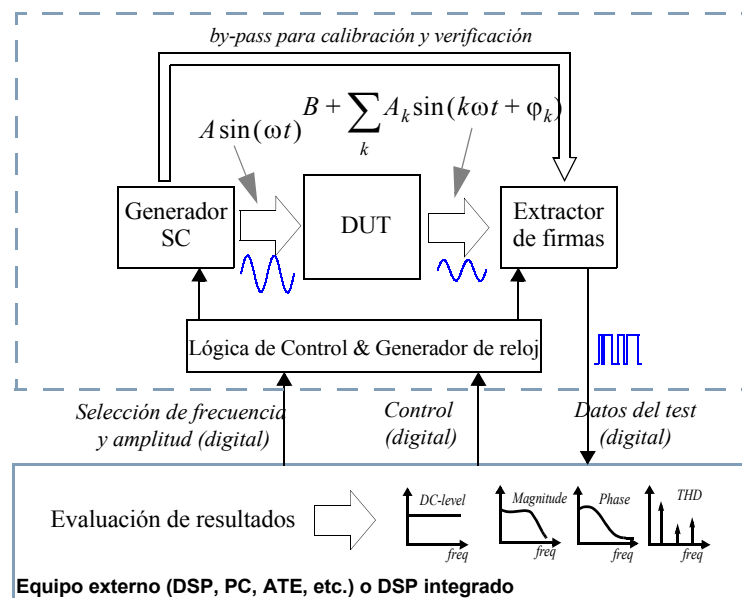
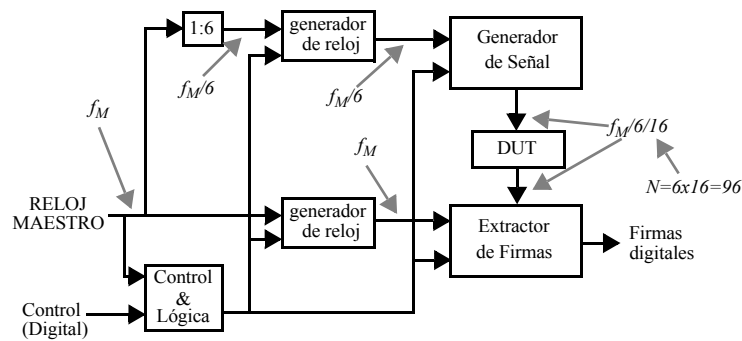


FIGURA 30. Ejemplo de sincronización entre generación y evaluación de señal



- El sistema para la caracterización de señales analógicas periódicas basado en una técnica de doble modulación, cuadrada y sigma-delta, también presentado anteriormente.

- Un bloque de lógica de control, encargado de la generación del reloj de cada bloque, mantener el sincronismo entre los diferentes bloques de test y proporcionar un interfaz digital con el equipo de test externo.

El camino de calibración en la Figura 29 tiene una doble función: hace posible la verificación de la circuitería de test y también permite la caracterización de la señal de test. Este último punto es fundamental en la operación de un analizador de redes. Dado que su funcionalidad requiere relacionar las señales de entrada y salida, es necesario entonces caracterizar tanto el estímulo de test como la respuesta al mismo.

En la operación del sistema, primeramente el estímulo de test generado por el bloque generador se pasa directamente al bloque analizador para calibración y autotest del sistema. Entonces, tras seleccionar la frecuencia y amplitud del estímulo de test, la lógica de control configura el generador de señal para llevar la señal de test deseada al DUT. La respuesta del DUT es analizada por el bloque de análisis de señal, que genera dos firmas digitales que codifican los parámetros característicos de la señal de respuesta. Finalmente las firmas obtenidas son procesadas y relacionadas con los valores de referencia previamente obtenidos en la fase de calibración para extraer la medida deseada (offset, ganancia, retraso, desfase, etc.).

Una característica importante del sistema de test propuesto es la sincronización inherente entre el generador de señal y el analizador de señal cuando se usa el mismo reloj maestro para generar los relojes y señales de control de ambos bloques. Como se muestra en la Figura 30, se emplea un reloj maestro a frecuencia  $f_M$  para generar directamente los relojes y señales de control del bloque analizador. Para generar los relojes y señales de control del bloque generador se utiliza un divisor entre seis para conseguir un sexto de la frecuencia del reloj maestro. Dado que el generador produce

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una señal a un dieciseisavo de su frecuencia de reloj, esto significa que el sobremuestreo en el analizador se fija a  $N = 6 \times 16 = 96$  por construcción.

### 3.2. Resultados experimentales

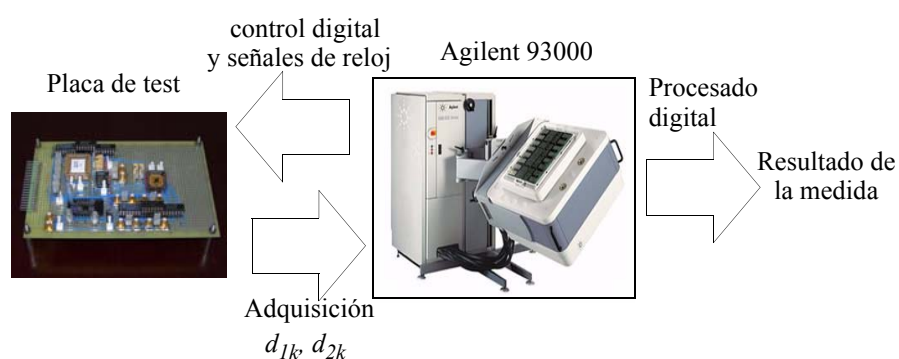
Los prototipos integrados del generador SC de señales sinusoidales y del analizador de señales periódicas, presentados y caracterizados en secciones anteriores, se han montado sobre una placa para implementar un prototipo del sistema de test propuesto en la Figura 29. En la misma placa se ha incluido además un filtro diferencial activo paso de baja de segundo orden, con una frecuencia de corte alrededor de 1kHz, que se utilizará como DUT.

El montaje experimental se ha esquematizado en la Figura 31. Se hace uso del sistema de test Agilent 93000 para generar las señales digitales de control y los relojes necesarios para la operación del sistema y también para la adquisición y procesado de las firmas digitales para la extracción de las medidas. Adicionalmente, se dispone de un generador de funciones arbitrarias y un osciloscopio digital comerciales para comparar las medidas.

Para probar la funcionalidad del sistema de test como analizador de redes, se ha caracterizado la respuesta del DUT seleccionado en términos de magnitud y fase. Las medidas se realizaron tomando 200 periodos para la evaluación. La Figura 32 muestra los diagramas de Bode de magnitud y fase obtenidos. La banda de error, en rojo en la figura, se ha calculado de acuerdo a la ventana esperada definida por (30) y (31). Las estrellas en azul marcan cada medida, mientras que la línea continua en verde muestra las medidas realizadas con el generador y osciloscopio externos. El acuerdo entre ambas medidas es muy bueno.

La Figura 33 muestra la funcionalidad del sistema como analizador de espectros. Esta figura muestra la estimación de la magnitud del segundo y tercer armónico en la salida del DUT, cuando la

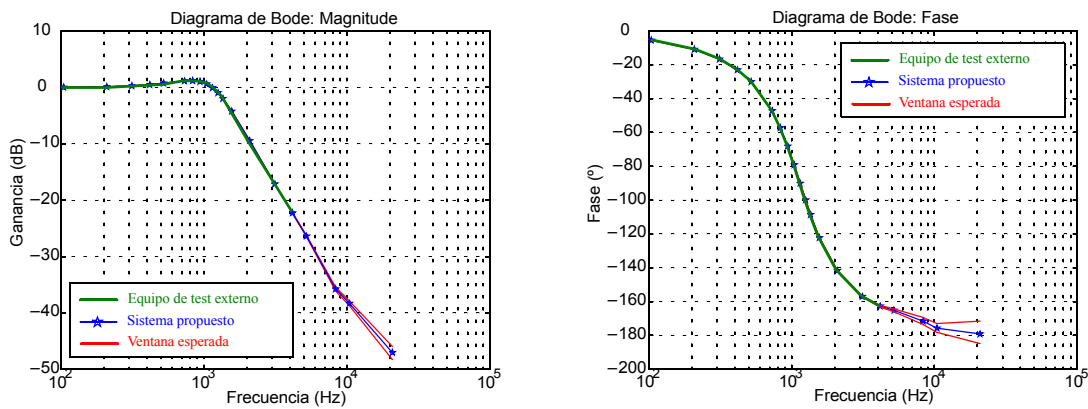
**FIGURA 31. Montaje de test**



señal de entrada es una senoide de 800mVpp, a 1.6kHz y a 1.3kHz. La línea azul representa las medidas del espectro realizadas con el osciloscopio digital comercial y el generador externo. El acuerdo entre ambas medidas es excelente. Además, si se requiere una mejor precisión, se puede conseguir aumentando el número de periodos de evaluación.

Las medidas de offset quedan demostradas en la Figura 34. Se ha medido el offset a la salida del DUT en el rango de frecuencia de interés. La línea continua marca la medida de este offset realizada con los equipos externos. El acuerdo entre ambas medidas es muy bueno.

**FIGURA 32. Medida del diagrama de Bode**



**FIGURA 33. Medidas de distorsión armónica: a) Frecuencia del tono principal = 1.6kHz; b) Frecuencia del tono principal 1.3kHz**

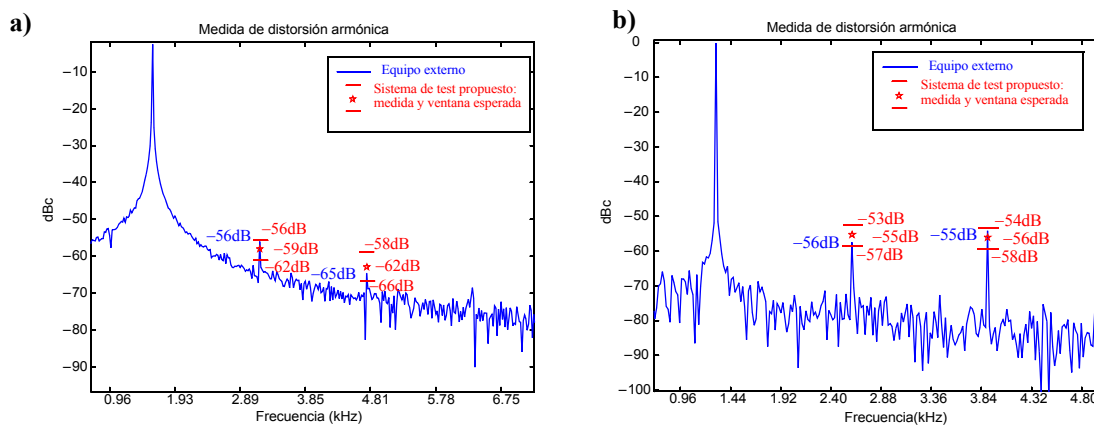
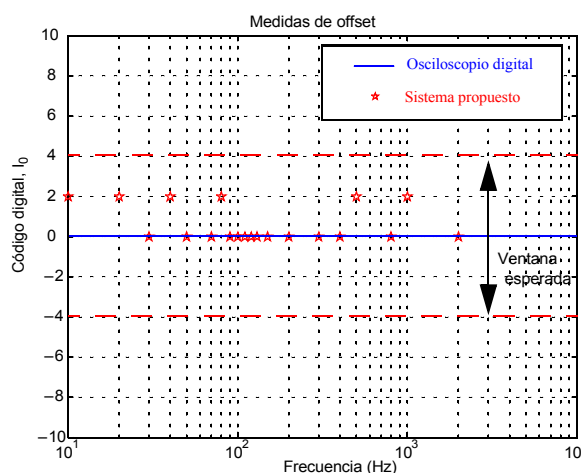




FIGURA 34. Medidas del offset del filtro




## 4. Conclusiones

Trasladar los equipos de test al propio chip que se quiere testar se ha convertido en la actualidad en una de las propuestas más atractivas para reducir la complejidad y el coste asociado al test de los subsistemas analógicos y de señal mixta inmersos en sistemas complejos. El desarrollo de bloques on-chip simples y reusables para funciones de test es uno de los pasos clave que posibilitan el empleo de esquemas BIST en tales sistemas. En esta línea, la principal contribución de esta tesis es el desarrollo y validación experimental de nuevas estrategias para la generación y caracterización on-chip de señales de test analógicas.

El esquema de generación de estímulos de test propuesto es adecuado para la generación de señales monotonaes con una alta pureza espectral, manteniendo unos bajos requerimientos de área y esfuerzo de diseño. El generador presentado se reduce principalmente a un filtro de bajo orden cuyos elementos de entrada han sido ligeramente modificados. Además, el generador puede ser controlado a través de un interfaz puramente digital, permitiendo la programabilidad de la frecuencia y la amplitud de la señal de entrada de una manera sencilla.

Por otra parte, el método de caracterización de señales analógicas que se ha presentado es adecuado para la caracterización completa de señales analógicas periódicas limitadas en banda y permite la extracción, en el plano digital, de su nivel de dc así como la amplitud y la fase de sus componentes armónicas. El método propuesto está basado en una aproximación de la serie de



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Fourier y su implementación se basa en una doble modulación, cuadrada y  $\Sigma\Delta$ , junto con un bloque muy simple de procesado digital.

Ambas propuestas han sido validadas no sólo desde el punto de vista teórico, sino que además se han mostrado resultados experimentales que las apoyan. En este sentido se han diseñado y fabricado en silicio varios prototipos de los bloques de test propuestos. En particular se han desarrollado dos generadores de señales sinusoidales, uno basado en la técnica SC y otro en la técnica OTA-C, y un prototipo del analizador de señales, todos ellos fabricados en una tecnología CMOS estándar. Multitud de resultados experimentales recogidos en esta tesis detallan el funcionamiento de los prototipos.

Finalmente, como una prueba de concepto se ha presentado un sistema de test completo que combina el generador y el analizador de señales desarrollados sobre una placa de test. Las medidas realizadas en el laboratorio demuestran que dicho sistema es capaz de caracterizar el comportamiento en frecuencia de un sistema analógico en términos de magnitud y fase, incluyendo también medidas de distorsión armónica y offset.

La simplicidad de los bloques de test propuestos, unida a la robustez de la circuitería empleada, su bajo esfuerzo de diseño y su interfaz puramente digital, los hacen muy adecuados para su empleo en aplicaciones BIST de circuitos analógicos y de señal mixta.

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## Conclusiones




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Trasladar los equipos de test al propio chip que se quiere testar se ha convertido en la actualidad en una de las propuestas más atractivas para reducir la complejidad y el coste asociado al test de los subsistemas analógicos y de señal mixta inmersos en sistemas complejos. El desarrollo de bloques on-chip simples y reusables para funciones de test es uno de los pasos clave que posibilitan el empleo de esquemas BIST en tales sistemas. En esta línea, la principal contribución de esta tesis es el desarrollo y validación experimental de nuevas estrategias para la generación y caracterización on-chip de señales de test analógicas.

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It is not necessary to mention that electronics plays a key role in our world. We can find integrated circuits almost everywhere, and they fulfil a lot of different tasks both in the industry and in our current day life. Electronics is now present in almost any human activity.

This evolution of electronics has been maintained over the last decades thanks to the IC industry efforts to further increase the capability of integration, struggling to follow the exponential evolution described by Gordon Moore back in the mid-60s [1]. Just to give some numbers, in 2004 according to the Semiconductor Industry Association (SIA) [2], the semiconductor industry manufactured more transistors than the global production of grains of rice, and at a lower production cost.

However, this exponential evolution is not free of shortcomings. Production costs have to remain bounded, but the ever increasing complexity of ICs is also increasing a component of the production cost at a rate that is not sustainable anymore. This component is the cost of circuit testing [3]-[5].

## 1.1. General thoughts on test

Testing an IC can be defined as the process of verifying if a given IC meets its intended specifications [6]. Just as any other industry, the evolution of electronics is driven by the competition to offer more value for less money to the potential customer. The mission of IC test within this picture is to screen defects, in such a way that manufacturers can warrant the performance of their products to their customers. An integrated circuit is just a small piece of silicon that has been crafted according to a certain layout to accomplish a given functionality. A defect is whatever causes a deviation in the physical chip beyond the normal variations of the fabrication process. Defects can have very different consequences in the functionality of the circuit. They may be harmless (like a change in a clear part of the layout), cause a permanent modification of the layout (like a short or an open), or even keep latent and manifest themselves during the life-cycle of the circuit (like an oxide pinhole causing an oxide breakdown).

In the end, IC testing is driven by end-user considerations. Customers will buy a certain IC based on a data sheet that states a certain functionality which accomplishes their needs. Translated to the IC testing paradigm, manufacturers must check the stated functionality before shipping the IC. The obvious option is to measure the performance of the circuit and compare it with the intended one. This testing scheme is known as functional test. On the other hand, other option is to measure the presence or not of defects in the circuit. Given that a defect-free circuit should fulfil its expected functionality by design, always inside the box of normal process variations, then detecting somehow the defects in a given IC is also a valid way of warranting its functionality. This approach receives the name of structural test [7]-[9].

Functional and structural tests both have their advantages and disadvantages. At first sight it is logical to think that the best and most direct way to check the specifications of a given circuit is by measuring them. However, a functional measurement implies that the test equipment must outperform the circuit under test (CUT), and besides that, it only measures the specifications at a given instant, while they have to be warranted over time. On the other hand, to state that a circuit is defect-free also ensures its functionality, but, actually, it is almost impossible to search and detect physical defects over a chip. Instead of that, defect-oriented tests search their manifestations at circuit level, that is, the faults they cause. Therefore, structural tests are always associated to a statistical level of confidence related to the number of faults that can be detected by the given test.

Structural test schemes have been widely accepted by the industry for the test of digital ICs. There are a number of reasons for that. A strong reason is that nowadays there is no alternative. A functional validation of a complex digital system would take too much time to test all the possible inputs. For instance, a combinational circuit with 100 inputs would take about  $4 \cdot 10^{12}$  years to test the possible  $2^{100}$  combinations at 10GHz (NASA's Wilkinson Microwave Anisotropy Probe project

[10] estimates the age of the universe to be  $13.73 \cdot 10^9$  years), and the situation is even worse for sequential circuits.

Historically, particle contamination during the fabrication process has been considered the main source of defects. This particle contamination may cause spots of additional or missing material across the different layers of the IC. From a circuit level point of view, this may translate to changes in the topology of the circuit due to shorts or opens. Although considering only spot defects is not enough for current deep submicron technologies, the focus of the manufacturers on spot defects has led to the successful stuck-at (one or zero) and stuck open fault models in digital circuits. The success of these models for digital testing is due to two main reasons. One of them is that there are tools to evaluate the fault coverage of the test, that is, it is possible to quantify its quality. The other reason is that they are the base of some generic, reusable and well established structural test techniques. Thus, we can find Automatic Test Pattern Generators (ATPGs) that can generate input sequences to maximize the detection of faults in a given circuit [11]-[13], a standard test bus, formalized in the IEEE 1149.1 and IEEE 1149.6 standards [14]-[15], to improve the accessibility and observability of digital circuits, and also Built-In Self-Test (BIST) techniques are available to include the test resources into the chip [16].

On the other hand, the analog and mixed-signal test paradigm is completely different [17]-[20]. Preferred solutions focus on the direct measurement of the performance parameters rather than in fault models. In fact, the difficulties in analog tests are given by the performance that have to be achieved and not by the complexity of the circuit functionality. And while it is still possible to find industrial test equipment that outperform the CUT, a functional approach will be preferred by the industry. There are many reasons for that. An important one is that the customer feels more comfortable with functional testing. Also, analog fault models are not as developed as their digital counterparts. There are intents to extend the standard digital test bus to the analog test domain [21]-[25], and it is still an issue to define a reusable fault model, compute its corresponding fault coverage, and define reliable fault detection techniques for the test of analog systems [26]-[34]. BIST schemes are also lagging.

Quoting the 2007 International Technology Roadmap for Semiconductors (ITRS) [35], no proven alternative to performance-based analog testing exists and more research in this area is needed. Analog BIST has been suggested as a possible solution and area for more research. Fundamental research is needed to identify techniques that enable reduction of test instrument complexity or elimination of the need for external instrumentation.

## 1.2. Test needs and DfT techniques along an IC life-cycle

The different test needs of a given IC are strongly application-specific. However, they can be described similarly across the IC life-cycle [7]. From the design board to the in-field operation of the system, each stage in the life-cycle of an IC has different test needs that have to be carefully considered, since the cost of the test increases exponentially in each step. The clever introduction of design for test (DfT) methodologies in each stage may represent a significant saving in the test cost. There are many definitions of the concept of DfT [5], [19], [36]-[38]. In a broad sense, DfT techniques can be defined as any technique, procedure or strategy leading to an improvement in any of the aspect of the test of an IC [19]. In the following, the different test needs in each stage of the life-cycle of an IC will be briefly presented, together with the role that DfT may play in each stage.

### *a. Design*

Taking into account the test during the design stage does not only mean to include dedicated DfT structures. During the design stage the designer gains a valuable knowledge about the circuit that can be of interest for further exploitation. Actually, the designer has to set up simulation test-benches for validation purposes that could be adapted and reused in the following production stages to perform actual tests.

The introduction of DfT structures in the circuit demands an extra design effort, but may represent important cost savings in posterior stages. The development of systematic and reusable DfT approaches is a key point to reduce these extra design efforts.

### *b. Prototyping*

The goal of this stage is to fully characterize a first silicon prototype. Once the design has been completed, a small number of samples are fabricated and submitted for characterization. The design must fulfil the specifications within the normal variability of the process. Test time and complexity are not a major concern at this stage. However, if there are DfT diagnosis capabilities, it will help the debugging of the design.

### *c. Wafer probe*

Once the prototyping stage is completed after the necessary redesigning cycles, the circuit is ready to be sent to the production line. In this stage the test cost concerns are focused on production volume. Before wafer dicing, the circuits on the wafer are tested. Wafer probing is the process of electrically testing each die on a wafer. This is done automatically using a wafer probing system, which holds each wafer on a stable platform and drops a set of precision point needles on designated



probe pads on the die. The probe system is usually connected to an ATE which manages the electrical tests during probing. Electrical test may not be extensive. Probing must be able to check whether the dice on a wafer are functional and meeting critical electrical parameters and detect the major number of the defective parts before packaging. Given that packaging is an expensive operation, minimizing the number of packaged defective circuits is important to reduce production costs. However, testing capabilities are very limited at this stage due to the parasitics introduced by the probe. And besides that, test time must be as low as possible to keep a reasonable production line throughput. Hence, DfT schemes at this stage should focus on improving test time or test coverage.

*d. Package test*

After wafer dicing, each circuit is packaged, which allows to test them in conditions that are closer to their actual operation. The goal of this test is to detect the defective parts that were not detected during wafer probe and the parts that were damaged by packaging.

In this stage a handler takes the packaged devices from the line, and loads them into a socket on a custom designed test board, known as DUT board or load board, which acts as an interface to an ATE. The test concerns in this stage are the same as for wafer probe test in terms of test time and test coverage.

*e. Burn in*

Burn-in testing are performed to check the reliability of the devices. Burn-in test consists in testing the circuit under conditions that tends to accelerate the manifestation of latent defects. The circuit is operated at a temperature and polarization above the maximum specified. The effect is equivalent to an accelerated aging of the circuit.

*f. System test*

System test is the final test step before the product is shipped to the customer. The fabricated circuit is included in a complex system involving many different components and technologies (optics, sensors, MEMs, etc.). The goal of system test is to verify the functionality of the whole product, search for defective parts or parts damaged by system assembly, and replace them before shipping the product. At this stage, DfT structures at component level can help diagnosis and reduce test time.

*g. In-field test*

There are many applications where in-field testing is a very desirable feature. Applications that have to work in a harsh environment or applications whose failure may cause disastrous

consequences in fields like automotive, spacial applications, aeronautics, medical instrumentation, oilfield prospecting, etc. are possible candidates.

Performing in-field tests is usually troublesome. Normally, test equipment is not available in the field of operation, nor it is possible to bring it there or to implement it within the system. Some applications may even require that the operation of the system is not interrupted by the testing procedure. In this stage, dedicated DfT strategies are usually the only way to provide the in-field test functionality.

#### *h. Maintenance*

Although at first sight it seems to be similar to the in-field testing, in fact maintenance is a very different issue. The goal of the maintenance is not to verify the functionality of the system, but to diagnose which component of the system is failing to be able to replace it. Again, DfT can be very useful in this stage. In spite of the fact that test equipment is usually available for maintenance operations, the integration of DfT structures at component level can simplify the diagnosis and reduce the cost of the required equipment. Aeronautics and automotive industries are two examples of fields where maintenance costs are a great concern.

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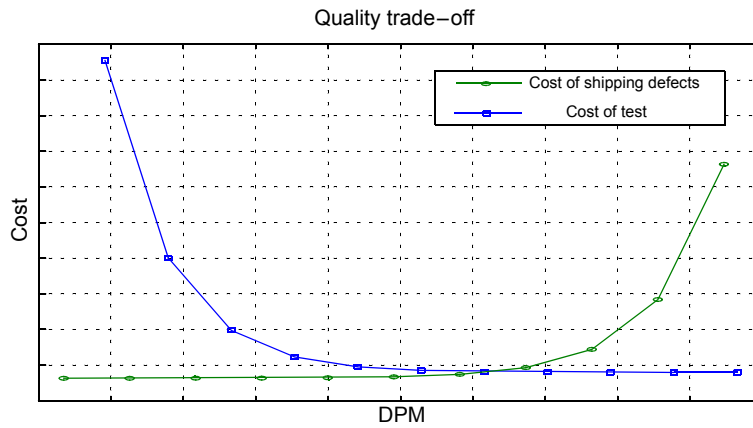
### **1.3. An analysis of the cost of test**

In the last years there has been a constant progress in the reduction of manufacturing test cost, enabled by advances in probe card technologies, new handling technologies, and innovative DfT techniques, however much work is still necessary. These improvements have been included mainly in logic test equipment, but significant work remains to translate similar capabilities to the analog, mixed-signal, and RF markets.

The acceptable cost of test is very market specific and must be determined by balancing the value of test with its cost. Figure 1.1 shows a typical curve that represents this test quality trade-off for an arbitrary chip. Normally, the cost of test increases exponentially with an improvement in DPM (Defects Per Million). Nevertheless, depending on the application, there may be test cost components that can not be easily calculated. For instance, the cost of shipping defective parts is not reduced to maintenance and replacement costs, but it may also affect the image of the manufacturer and make it lose part of its market share.

Generalizing, the capital cost of a test cell can be expressed in terms of the relevant cost drivers of future test technology [35] as,

FIGURE 1.1. Arbitrary example to illustrate the test quality trade-off



$$C_{CELL} = C_{BASE} + C_{INTERFACE} + C_{POWER} + C_{TEST-CHANNELS} + C_{OTHERS} \quad (1.1)$$

In this expression,  $C_{BASE}$  is the cost of a test system with zero pins or channels, that is, it includes the cost of the mechanical infrastructures, tester operating system software, and central instruments.  $C_{INTERFACE}$  includes the costs required for interfacing with the device, for instance, the cost of interface electronics, sockets, and probe-cards.  $C_{POWER}$  is the cost of the power supplies.  $C_{TEST-CHANNELS}$  is the cost of test instruments, such as digital, analog, RF, and memory test instruments.  $C_{OTHERS}$  includes any remaining costs, for instance, floor-space. Test scenarios are evaluated by dividing the capital cost and performance metrics. An important figure of merit is the Units per Hour per Cost (UPH/\$M), defined as the number of shipped devices per hour over the total cost.

The introduction of DfT techniques can reduce the cost components  $C_{INTERFACE}$  and  $C_{TEST-CHANNELS}$ . Thus, DfT adoption may reduce the ATE performance requirements and the number of needed test pins. DfT methodologies for analog and mixed-signal test are required. The relatively high cost of analog, mixed-signal and RF test instruments, and the long test times associated with testing of these circuits are still key challenges. DfT methodologies are also a solution to control the interface costs. This is essential for successful cost scaling using multi-site testing: a dominating interface cost that increases exponentially with the number of sites may defeat the purpose of increasing the number of test-sites. However, it is important to notice that some DfT techniques also increase demand on power supplies, increasing the  $C_{POWER}$  cost components, but

normally the extra cost is mitigated by shorter test times that improve the Unit per Hour per Cost figure.

#### **1.4. A special case: DfT for analog and mixed-signal SoCs**

Over the past 25 years, semiconductor industry has been driven primarily by increasing performance and transistor counts. However, a fundamental change is in process due to new market demands, such as mobility, security, ease of use, low power, etc. This is driving the integration of different semiconductor technologies in more ways and in a greater set of applications than ever before. This in itself represents a huge challenge to test. The integration of very heterogeneous technologies, that in the recent past have demanded different test solutions and specific equipment and interface tools, makes necessary a clever DfT strategy. Indeed, a successful integration is determined not just by “can it be done?” but also by “can it be tested economically?”

A SoC (System on Chip) design consists of multiple individual design blocks, or cores, using different technologies (logic, memory, analog, mixed-signal, RF, etc.), integrated on a single substrate. SoC designers are forced to use pre-existing IP cores that includes the design itself, its embedded test solution, and the needed interface to other cores. This implies that a highly structured DfT infrastructure is needed to observe and control individual test core solutions. DfT must contemplate the appropriate combination of tests for individual cores, the test core access, and full-chip testing.

The ITRS identifies the need to combine test requirements from multiple sources with different testability methods as one of the fundamental challenges of SoC test. For instance, if there are a high speed logic core and a high resolution analog to digital converter, then an ATE with both capabilities would be necessary. Accessibility and observability of internal nodes are also a problem in a highly integrated system. Digital cores usually include test solutions like boundary-scan or digital BIST, but if an embedded analog circuit has to be functionally tested, these standard solutions do not exist. For instance, if an analog stimulus is required to perform a functional test of a given analog core, the stimulus has to be, somehow, either carried from one of the SoC pads, or internally generated somewhere inside the SoC and communicated to the analog core under test. Furthermore, the circuit added for such purposes should not significantly impact the yield.

In this line, the ITRS sketches some research areas for successful DfT structures for analog and mixed-signal cores:

*a.* Enhancing accessibility and observability

In a tightly integrated SoC, the internal nodes of the circuit, and even the inputs and outputs of most of the cores composing the SoC, are not directly accessible from the SoC pads. It is necessary

to develop a structured methodology to provide test stimuli to different nodes within the SoC, and/or to monitor a given node. The IEEE 1149.4 analog test bus standard is an advance in this line, but further research is still needed.

*b.* Moving some of the test equipment on-chip

By moving some of the test equipment to the chip, it would be possible to relax the specifications of the ATE and the test interface. The addition of some test functions such as test stimulus generation, response extraction, test control, etc. within the chip would indeed relax the tester and its interface. However, it is a challenge to include high quality instrumentation on-chip, and the added cost must be low to make this approach viable.

*c.* Develop reusable BIST schemes

Built-in self-test schemes are the natural extension of the previous point. Ideally, these test schemes includes all the needed resources to perform the test. They only require a external control signal and a power supply. Test stimulus generation, data acquisition, test interpretation, and test control are performed on-chip. This may represent dramatic savings in the cost of the test equipment. Indeed, a circuit featuring a BIST scheme may be tested with low cost test equipment, that only has to provide clocking, power supply, and a low speed I/O interface. In addition, the introduction of BIST techniques within the different cores composing a SoC may enable massively parallel measurements, that can reduce drastically the test time.

In a futuristic scenario, each of the different blocks that compose a mixed-signal SoC will have an embedded BIST solution that will only require a digital signal to start the test, and will output a digital “go/no-go” signal. The digital start signals will be fed to each block in the SoC by a standardized test interface such as the cited IEEE 1149.1 test bus, that will also get the test output signals.

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## **1.5. The work in this thesis: on-chip generation and characterization of analog signals for BIST applications**

As mentioned before, analog/mixed-signal BIST solutions have been proposed as a way to improve testability while reducing test cost. BIST techniques are based on including test resources on-chip, together with the device under test (DUT). Summarizing, an efficient BIST approach should have the following features:

- Low speed digital interface needs with ATE for control and synchronization tasks. In this way, low cost digital ATEs can be used.
- Programming capabilities to accommodate the test program to the target measurements.
- Robustness against environmental noise and process variations.
- Low design effort and area overhead.

This thesis presents methodologies for the on-chip generation and characterization of analog signals that accomplishes the previously cited features, and therefore, are very suitable for its inclusion within a BIST scheme for analog and mixed signal cores. Analog and mixed signal testing schemes make use extensively of analog signal generators and signal characterization equipment, so providing efficient methods for the inclusion of this instrumentation on-chip is one of the key points to move many testing schemes to a full-BIST structure.

This thesis memory is organized as follows.

Chapter 2 proposes a new method for the on-chip generation of analog sinewave signals with reduced circuitry requirement and high spectral purity, maintaining the attributes of digital control, programmability and robustness as demanded for BIST applications. The proposed approach is analytically validated, and its implementation and theoretical performance are widely discussed.

Chapter 3 presents the design of two integrated prototypes of the signal generator, namely a continuous-time generator and a discrete-time one, and experimental results are given to support the proposed approach.

Chapter 4 presents a novel methodology for the evaluation of periodic analog signals suitable for on-chip implementations. Again, a mathematical discussion validates the proposal, and its implementation and expected performance are detailed.

Chapter 5 describes the design of an integrated prototype of the proposed signal characterization block. Experimental results are given to validate the proposal.

Chapter 6, as an example application, presents a test core featuring both the generator and the evaluator block presented in the previous chapters. The proposed test scheme can cope with the frequency response, both magnitude and phase, harmonic distortion, and offset measurements of an analog circuit. A demonstrator board is presented, featuring the proposed test core and a filter as a DUT, and experimental results are given to support its stated functionality.

Finally, Chapter 7 summarizes the key points of the presented works in the conclusions.

## On-Chip Analog Sinewave Generation

*This chapter presents an analog sinewave signal generation technique with reduced circuitry resources. It is based on a modified filter that gives a sinewave signal in response to a DC input. The proposed architecture has the attributes of digital programming and control capability, robustness, low area overhead, and low design effort, what make it very suitable for BIST applications.*

## 2.1. Introduction

Test schemes for analog and mixed-signal functional testing require analog signal generators to provide a test stimulus. Analog signals such as ramps, sinewaves, triangular waves, etc., are some typical examples of analog signals widely used for testing purposes [40], [42]-[46], [48]-[52].

In this chapter, we are going to focus on the on-chip generation of analog sinewaves. This kind of signals has a wide variety of potential applications in the field of analog and mixed-signal testing and represents a key point in many testing schemes. In fact, most of the analog and mixed-signal subsystems in a SoC, such as analog filters, A/D converters, signal conditioners, etc, can be characterized by applying this test stimulus. For instance, frequency related specifications such as gain, delay, pass-band performance and stop-band edges, distortion, signal-to-noise ratio, dynamic range, etc. are typical performance specifications usually measured by applying sinewave stimuli to the circuit and evaluating the responses using appropriated processing algorithms. Testing A/D converters is another clear example. Many of the A/D converter performance specifications, such as code transition locations, harmonic and spurious distortion, noise figures and frequency response parameters, can be measured by applying sinusoidal stimuli. Indeed, the IEEE standard 1241-2000 [39] describes a wide set of standard test setups and test methods for the characterization of A/D converters based on the application of sinusoidal test signals and the evaluation of the responses through a proper processing algorithm.

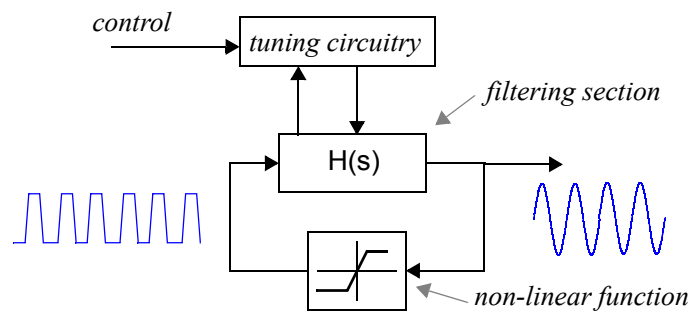
This chapter is organized as follows. Firstly, Section 2.2 reviews briefly different techniques previously reported for the generation of analog sinewave signals. Section 2.3 details our proposal and analyzes its main advantages and limitations. After that, Section 2.4 discusses different design techniques for the implementation of the proposed generation scheme. Finally, Section 2.5 summarizes the key points of the chapter.

## 2.2. Review of previous techniques

A classical solution for the on-chip generation of sinewave signals is the analog oscillator based on a non-linear feedback loop [41]-[44]. It consists of a filtering section and a non-linear feedback mechanism in the arrangement shown in Figure 2.1. The non-linear feedback block forces the oscillation at a given frequency, while the filtering section removes the unwanted harmonic components. The quality of the generated signal depends on the linearity and selectivity of the filter and the shape of the non-linear function, while the tuning of the filter allows the programmability of



FIGURE 2.1. Oscillator-based sinewave generator



the frequency. However, highly selective filters and smooth non-linear functions are needed for the generation of high-accuracy, low-distorted waveforms, what normally make its design a challenging task.

Commercial ATEs usually make use of a different generation scheme. Normally, they rely in a digital arbitrary waveform generator for the generation of analog test stimuli. These waveform generators (see Figure 2.2) are based on a digital pattern generator and a D/A conversion. The digital pattern generator outputs a digital sequence previously loaded in a digital memory, the D/A converter translates the digital pattern to the analog domain, and finally the signal is fed to an analog filter that attenuates all the non-desired components in the output signal. It has the advantages of a digital interface for control and programming tasks, and it also offers the characteristics of robustness and reusability that are common to the digital circuitry.

Most of the proposed strategies for on-chip generation of analog test signals adapt the digital scheme in Figure 2.2. A direct on-chip implementation for the generation of analog sinewaves is the ROM-based generator shown in Figure 2.3. The digital pattern generator is implemented using a ROM that outputs the stored samples of a sinewave, controlled by a digital counter. The accuracy of the signals generated by this setup is limited by a number of factors. In terms of frequency it is

FIGURE 2.2. Standard arbitrary waveform generation in commercial ATEs

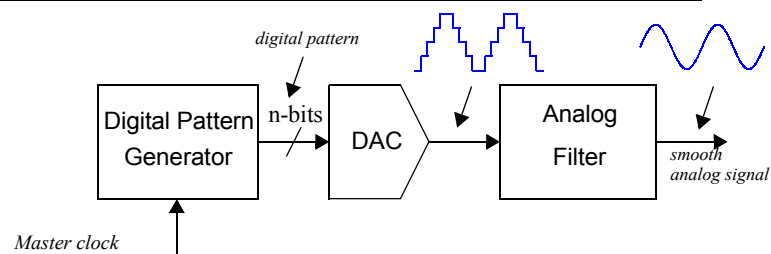
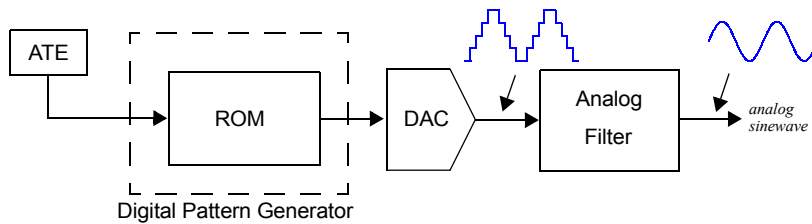


FIGURE 2.3. ROM-based sinewave generator



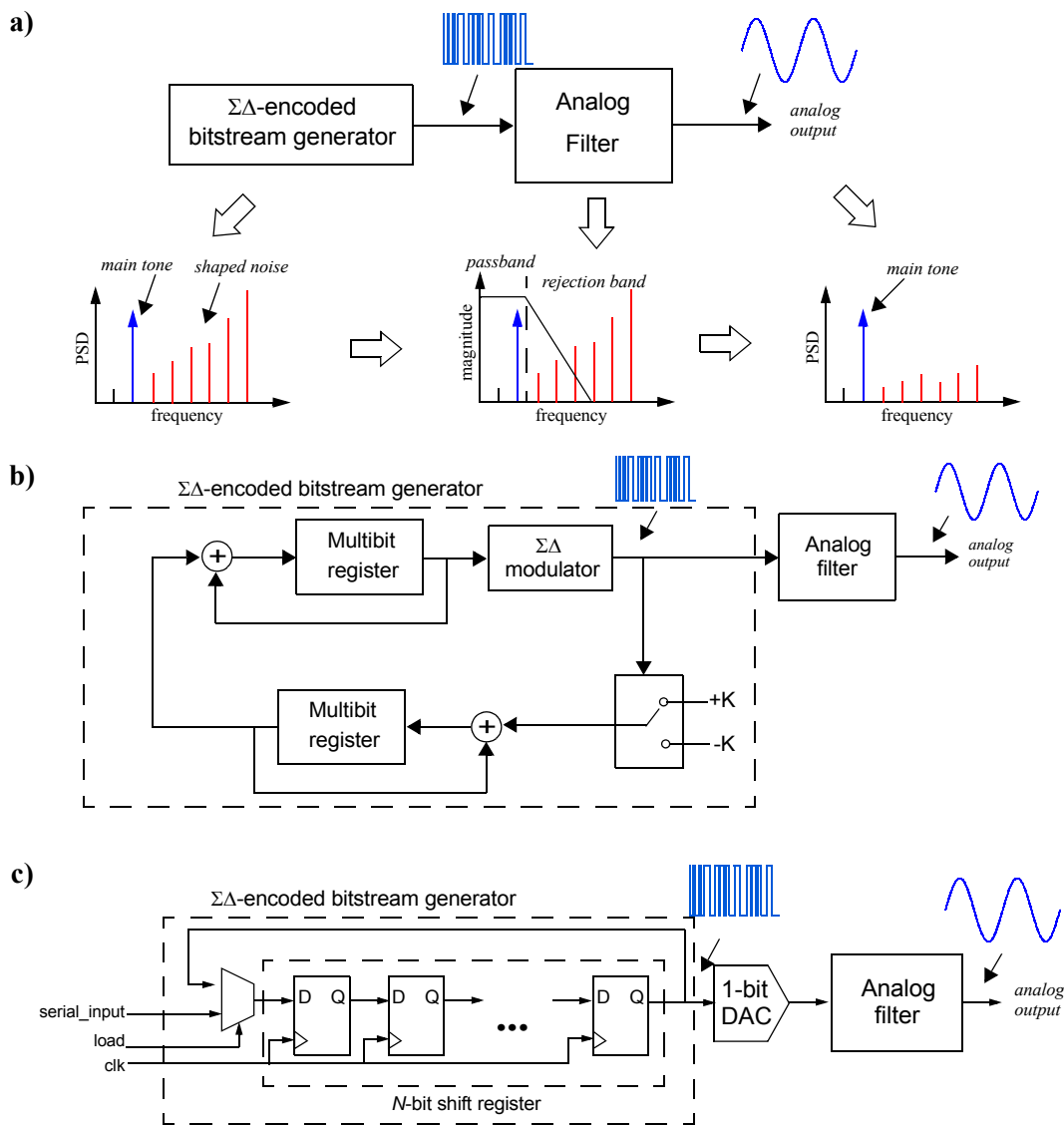
limited by the number of samples stored in the ROM, and in terms of spectral quality either by the word length of each sample, the characteristics of the D/A converter, or the performance of the output filter. The application of this technique within a BIST scheme is usually not practical unless the required circuitry is already available in the system and it can be reused during test mode. In other cases the needed circuitry may represent a large area overhead.

An alternative implementation for the digital pattern generator to overcome the limitations of the ROM-based approach in terms of area and signal quality is proposed in [45], and illustrated in Figure 2.4a. It is based on exploiting the noise-shaping characteristics of  $\Sigma\Delta$  encoding schemes [47]. Basically, its functionality consists of generating a 1-bitstream  $\Sigma\Delta$ -encoded version of an  $N$ -bit digital signal and matching the shape of the reconstruction filter with the noise shaping characteristics of the encoded bit-stream. There are two basic approaches to generate the 1-bit  $\Sigma\Delta$  encoded bitstream: a  $\Sigma\Delta$  oscillator and a memory-based signal generator. Both approaches can be implemented on-chip. However, although the first one achieves a better signal quality, the second one is more area efficient.

A  $\Sigma\Delta$  oscillator, such as the one shown in Figure 2.4b, consists of a digital resonator and a  $\Sigma\Delta$  modulator in a loop gain configuration. The digital resonator generates an  $N$ -bit sinusoidal signal, with amplitude and phase determined by the initial conditions stored in the multibit registers. The  $\Sigma\Delta$  modulator generates a 1-bit  $\Sigma\Delta$ -encoded version of the signal created by the resonator. The output analog filter is matched to the noise-shaping characteristic of the  $\Sigma\Delta$ -modulator to reject the shaped noise. High precision and high frequency resolution have been demonstrated with this approach [48], [49]. However this method presents some limitations: its design is not straightforward, its application is limited to single tone signals, and the reconstruction filter has to be highly selective to reject the noise (for instance, a 6th-order filter is used in [48]).

On the other hand, Figure 2.4c shows the memory-based approach [45]-[46]. The basic idea is to store and periodically reproduce a truncated 1-bit  $\Sigma\Delta$ -encoded version of an  $N$ -bit digital signal, using a feedback chain of memory elements. An analog reconstruction filter cancels out the non-desired frequency components. This approach has many interesting advantages.

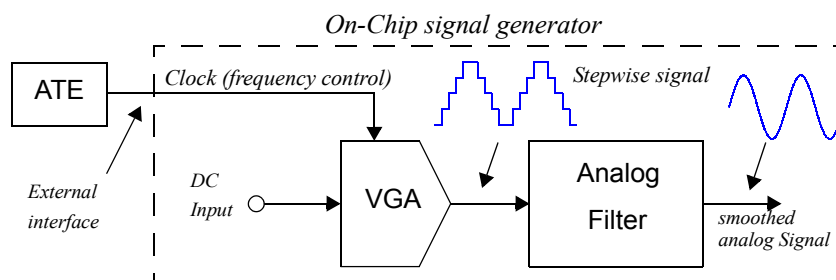
FIGURE 2.4. a) General block diagram of a signal generator based on  $\Sigma\Delta$ -encoding; b)  $\Sigma\Delta$  oscillator implementation; c) Memory-based implementation



Single-tones with a high spectral quality can be obtained, but this technique is not restricted to single tones. On the contrary, arbitrary band-limited multi-tone waveforms can be easily generated. Furthermore, the required circuitry is mostly digital, and concerning its area overhead in a practical BIST application, it can be greatly reduced if existing digital resources in the system, such as boundary scan chains, RAMs, etc, can be reused. The main limitations of this technique are that it requires large bit-stream lengths if both amplitude and frequency have to be accurately controlled [50], and also demands a highly selective analog filter, at least one order higher than the order of the  $\Sigma\Delta$  scheme used to generate the bitstream, to remove the noise. In addition, this approach is frequency limited due to the need of very high oversampling ratios.

A very simple scheme for discrete-time periodic analog signal generation can be found in [51]-[52]. It consists of a variable gain step-wise switched-capacitor (SC) amplifier (VGA) where each gain step represents a value of a sampled and held signal (a reset sets the zero of the signal). This scheme can be easily extended to the generation of continuous-time sinewave signal if needed, as depicted in Figure 2.5, introducing an output analog filter. The scheme in Figure 2.5 is in fact quite similar to that in Figure 2.2 if it is taken into account that the VGA and the digital control of the gain play the role of the D/A converter in Figure 2.2. In the case of a sinewave signal, the symmetry of the signal only need  $N/4+1$  gain steps to generate the signal with  $N$  steps per period, if  $N$  is a power of 2. The number of steps should be low, because otherwise the complexity of the logic and the area overhead increases drastically. The main advantages of the approach are that both the amplitude and the frequency of the signal can be easily controlled by a DC input voltage and the clock frequency respectively, which also ensures synchronism capability and programmability, together with the simplicity and robustness of the logic and the SC circuitry. In terms of spectral purity the performance is limited by the accuracy and number of the generated steps. Improving the performance would require the use of a very selective filtering stage, thus increasing the area overhead, to reduce the level of unwanted components.

**FIGURE 2.5. Variable-gain-amplifier-based sinewave generator**



The discussed approaches achieve the desired signal generation using a variety of different techniques. However, it is also certain that some elements are common to all of them. From the previous review of different generation techniques, it can be inferred that:

- Both analog approaches and digital generators make use of analog filters to smooth the output signal, attenuate all the non-desired frequency components and, in the digital case, reconstruct the analog signal after the D/A interface. This analog output filter is essential for the generation of single-tone analog sinewaves, where a given spectral purity has to be assured.
- Focusing on digital-based generators, which are usually the preferred solutions, the unavoidable output filter must match the linearity of the previous digital circuitry in the generation chain. Otherwise, the linearity of the filter will limit the performance of the generator. The analog output filter effectively limits the maximum achievable performance of the whole system.
- The output filtering stage becomes a key element in these generation schemes.

### 2.3. Proposed approach for sinewave generation

In this section, a novel technique suitable for the on-chip generation of analog sinewave signals is introduced. The main idea consists of merging signal generation and filtering in a single linear system similar to the output analog filter employed in all the previously discussed generation approaches. This way, the proposed approach reduces drastically the overhead, while, as it will be demonstrated later in this chapter, it maintains the attributes of robustness, digital control, and programmability for accommodating the generated signals to the desired test tasks.

#### A. Theoretical basis

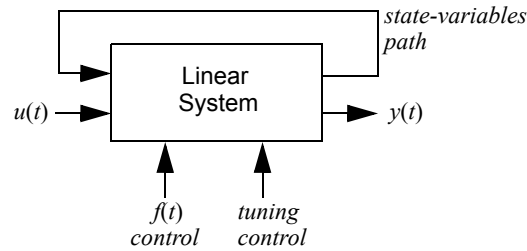
First of all, it is convenient to remark that although the discussion will be restricted to the continuous-time domain, it can be straightforward extended to the discrete-time case.

Let be a  $n$ -th order linear system with one input,  $u(t)$ , and one output,  $y(t)$ , described in terms of its state variables,  $[x(t)]$ , as,

$$\begin{aligned} [\dot{x}(t)] &= [a][x(t)] + [b(t)]u(t) \\ y(t) &= [c][x(t)] + d(t)u(t) \end{aligned} \quad (2.1)$$

where  $[x(t)]$  is an  $n \times 1$  column vector, coefficient  $[a]$  is an  $n \times n$  matrix, coefficient  $[b(t)]$  is an  $n \times 1$  column vector, coefficient  $[c]$  is a  $1 \times n$  row vector, and coefficient  $d(t)$  is a scalar function. Coefficients  $[b(t)]$  and  $d(t)$ , that represent the dependence of the state variables  $[x(t)]$  and the output  $y(t)$  with respect to the input  $u(t)$ , are time dependent.

FIGURE 2.6. Conceptual diagram of the proposed generator



Let us consider the particular case,

$$\begin{aligned} [b(t)] &= [b]f(t) \\ d(t) &= df(t) \end{aligned} \quad (2.2)$$

where  $[b]$  and  $d$  are constants and  $f(t)$  is a time-dependent function. Figure 2.6 shows a conceptual diagram of the described system, in which the external controls over the tuning and the  $f(t)$  have been included. Using the Laplace Transform, it can be shown from (2.1) that,

$$\begin{aligned} Y(s) &= H(s)\{F(s) \otimes U(s)\} \\ y(t) &= h(t) \otimes \{f(t)u(t)\} \end{aligned} \quad (2.3)$$

where capital letters denote the Laplace Transform, operator  $\otimes$  represents the convolution product,  $H(s)$  is a transfer function of value,

$$H(s) = [c]\{s[I] - [a]\}^{-1}[b] + d, \quad (2.4)$$

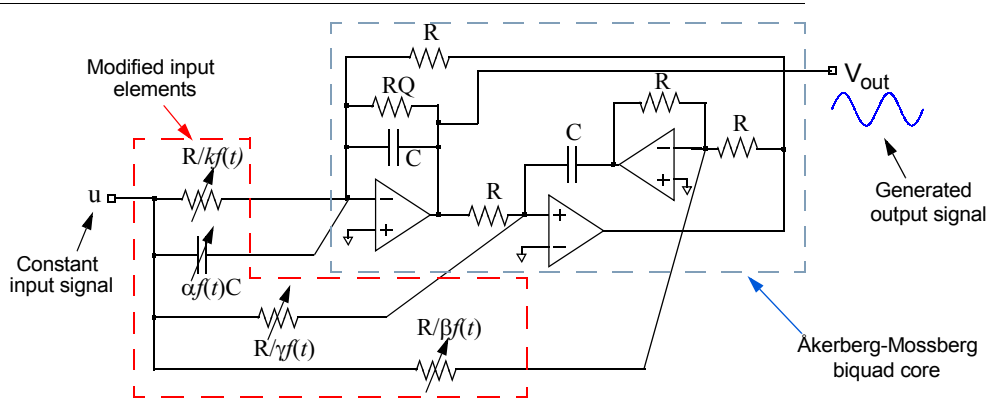
where  $[I]$  is the  $n \times n$  identity matrix, and  $h(t)$  is the Inverse Laplace Transform of  $H(s)$ .

From (2.3) it is clear that the system described by (2.1) performs, in the most general case, the filtering of the product  $f(t)u(t)$  accordingly to the impulse response given by  $h(t)$ . The system acts as a multiplier and a filter all in one.

Restricting the discussion to its use as a signal generator (the use as a multiplier, although interesting, is out of the scope of this thesis), let us consider the particular case  $u(t) = u$ , where  $u$  is a constant value. Then, the output of the system can be rewritten as,

$$\begin{aligned} y(t) &= h(t) \otimes \{u \cdot f(t)\} = u \cdot \{h(t) \otimes f(t)\} \\ Y(s) &= uH(s)F(s) \end{aligned} \quad (2.5)$$

FIGURE 2.7. Åkerberg-Mossberg circuit-based example



Under these conditions, as a response to a constant input, the system delivers an output signal  $y(t)$ , which is the function  $f(t)$  filtered accordingly to the transfer function  $H(s)$  and scaled by a factor  $u$ .

At this point, if  $f(t)$  is a periodic function, then the system will output also a periodic signal. If the transfer function  $H(s)$  removes all the non-desired frequency components, this periodic output will become a sinusoidal-like waveform.

It is important to notice that the amplitude and frequency of the generated waveform can be programmed. The scaling factor  $u$  (the constant input of the system) controls the amplitude of the output signal, and function  $f(t)$  together with the tuning of the system transfer function control its frequency.

Figure 2.7 shows a conceptual example of realization of the proposed system to illustrate the described approach with a simple particular case. The system in Figure 2.7 is a general biquad based on the well-known Åkerberg-Mossberg circuit [53], whose input devices have been replaced by time-dependent elements. The response of this system at node  $V_{out}$  to a constant input  $u$  is described by (2.5), where the transfer function  $H(s)$  in the Laplace domain is given by,

$$H(s) = -\frac{\alpha s^2 + s\omega_0(k - \beta) + \gamma\omega_0^2}{s^2 + s(\omega_0/Q) + \omega_0^2} \quad (2.6)$$

and the central frequency  $\omega_0$  is defined by  $\omega_0=1/RC$ .

In the case that function  $f(t)$  is a periodic function and that the transfer function  $H(s)$  is properly tuned to remove the non-desired frequency components of  $f(t)$ , the system in Figure 2.7 represents an example of the described sinewave generator.

### B. The choice of the periodic function $f(t)$ and the transfer function $H(s)$

There are many potential candidates for function  $f(t)$ . In a first instance, any periodic function may be suitable from a theoretical point of view. However, the choice of  $f(t)$  in a practical case must be driven by two main factors:

- its ease of implementation within the particular system,
- the magnitude of its non-desired spectral components.

A trade-off arises between the shape of function  $f(t)$  and the spectral selectivity of the transfer function  $H(s)$ : the more similar function  $f(t)$  is to a pure sinewave in terms of spectral quality, the more relaxed the selectivity of  $H(s)$  can be made. Figure 2.8 shows some basic periodic waveforms

**FIGURE 2.8. Function  $f(t)$  examples: a) Sawtooth function; b) Square-wave; c) Triangular wave; d) Step-wise sinewave**

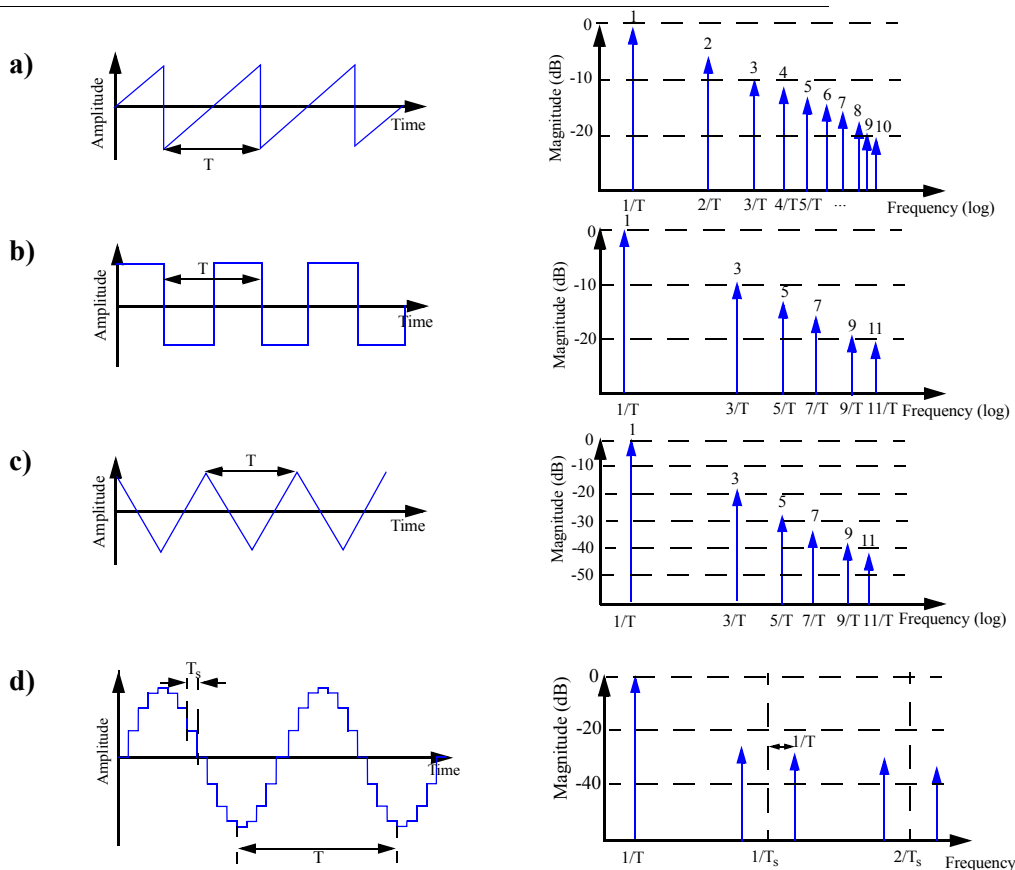
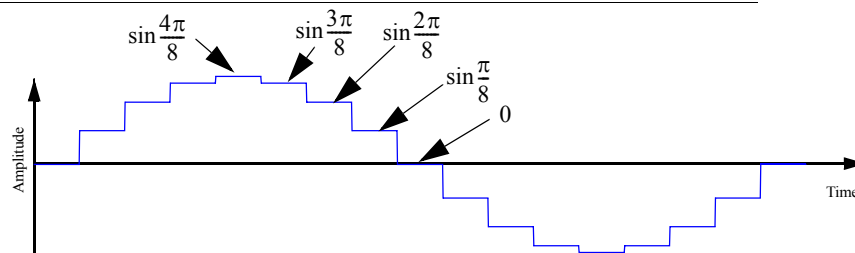




FIGURE 2.9. Example of a 16-step sinewave generated from 5 different values



and their spectra. For instance, if  $f(t)$  is a sawtooth waveform, the needed filtering will be more selective to get a given spectral purity than if a triangular wave is used instead.

Step-wise sinewaves offer a good trade-off in this sense and for this reason in the following we are going to focus the discussion on this kind of functions. Their spectra are essentially the same of a sampled sinewave, but modulated by a sampling function. Even with a relatively low number of step levels, the magnitude of the unwanted components is lower than in the other considered choices, which allows to relax the  $H(s)$  selectivity. In addition, due to the symmetry of the sinewave functions if the number of step levels is a power of two,  $2^L$ , then only  $2^{L-2}+1$  different values describe the complete waveform (see the waveform example in Figure 2.9).

The practical realization of  $f(t)$  as a step-wise sinewave also offers advantages in terms of simplicity. Step-wise variation of the input devices of a system can be achieved simply by using digitally controlled device arrays. For instance, recalling the example in Figure 2.7, the time-dependent input devices can be implemented as illustrated in Figure 2.10 using digitally programmable resistors and capacitors to achieve the desired step-wise function  $f(t)$ . The variable input in this example has been set to generate the resistance and capacitance positive values for a 16-step sinewave, controlled by the digital waveforms shown in Figure 2.10c, while two input switches

FIGURE 2.10. Input devices for the example in Figure 2.7: a) Programmable resistor; b) Programmable capacitor; c) Control signals timing diagram

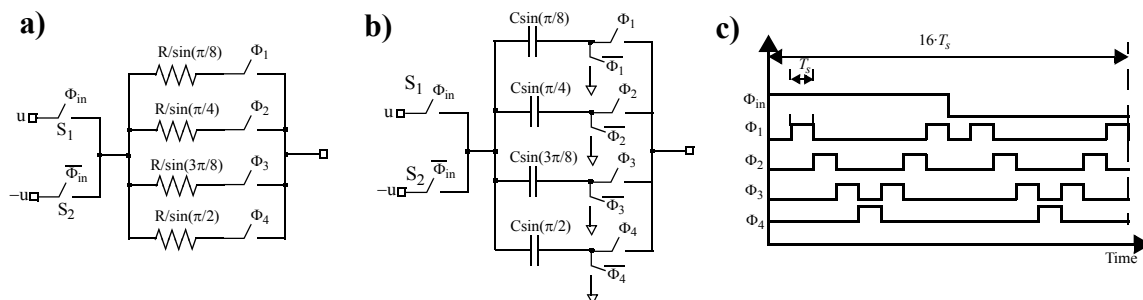
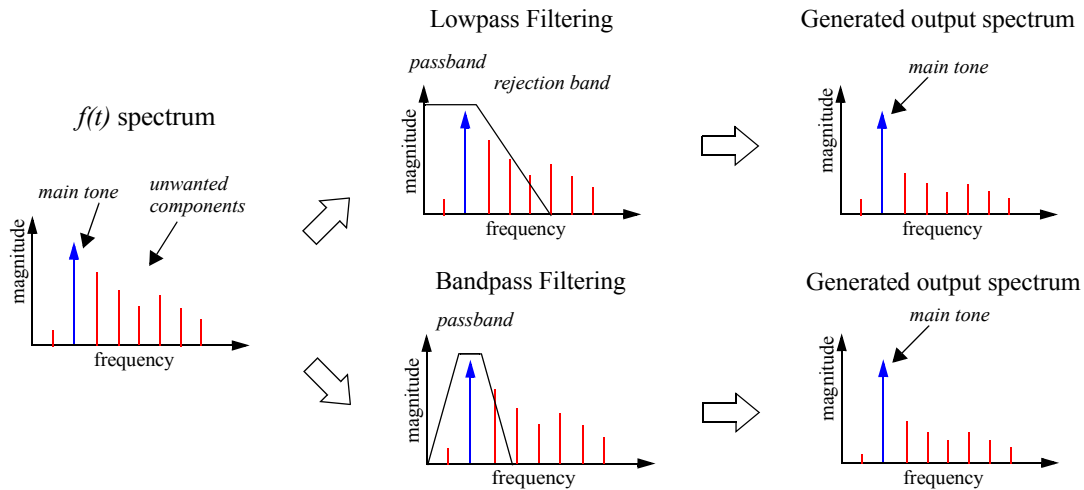


FIGURE 2.11. Matching the shape of the filter and the target waveform



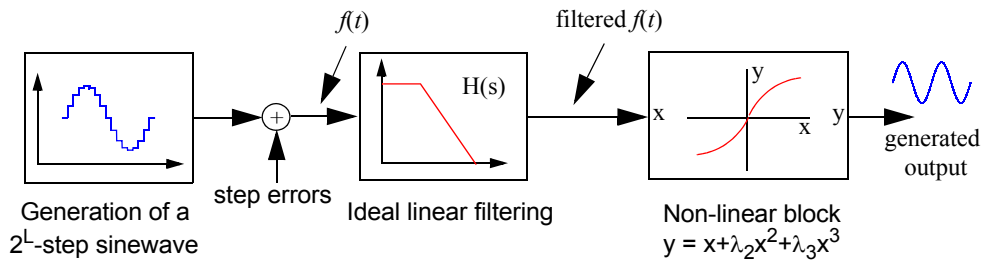
( $S_1$  and  $S_2$ , shared by all the input devices) set the weight (positive or negative) of each step. This strategy to build the  $f(t)$  function based on switching the input devices of a filter can be easily adapted to the most common integrated filter design techniques, such as OTA-C, MOSFET-C, or SC filters [54]-[58]. Two practical design examples (using the OTA-C and SC techniques) will be given in the following chapter.

Regarding the system transfer function, what is needed is to match it to the shape and frequencies of interest in the application. In this sense, lowpass and bandpass shapes are clearly the most convenient whenever the main harmonic of function  $f(t)$  is in the passband and the unwanted harmonics in the rejection band, as depicted in Figure 2.11

### C. Performance limits of the proposed approach

This section analyzes the performance that can be reached with the proposed strategy. For that, it is needed to make some considerations in order to be realistic in the analysis. Let us recall that the functionality of the proposed generation scheme is based on the variation of the input devices of a linear system with a certain transfer function  $H(s)$ , according to a periodic function  $f(t)$ , and excited by a constant input  $u$ . It has been demonstrated (see equation (2.5)) that, from the output point of view, such a system is completely equivalent to a system with the same transfer function  $H(s)$  excited by the signal defined by the product  $u \cdot f(t)$ . Consequently, it should be clear that the main limitations of the proposed approach are given by:

FIGURE 2.12. High level model of the proposed sinewave generation scheme



- The realization of function  $f(t)$ : restricting the discussion to the case of step-wise sinewaves, both the number of steps per period and the possible errors affecting these step levels will have a direct impact in the performance.
- The selected linear system: the shape of its transfer function  $H(s)$  defines the attenuation of the non-desired frequency component of function  $f(t)$ , while its non-idealities in terms of non-linear behavior will introduce distortion in the output signal.

Figure 2.12 shows a high level model which contemplates these limitations. The proposed model has three main blocks: an input block which generates the function  $f(t)$  (in the sake of simplicity, the scaling factor  $u$  has been considered to be unity), an ideal linear filter with transfer function  $H(s)$ , and a non-linear block which models the non-linearity of the system. It is important to notice that the analysis of other limiting factors, such as a noise analysis of the filter, is related to the particular implementation of the filtering stage, and not to the proposed generation scheme itself. Hence, the filter noise will not be considered at this level.

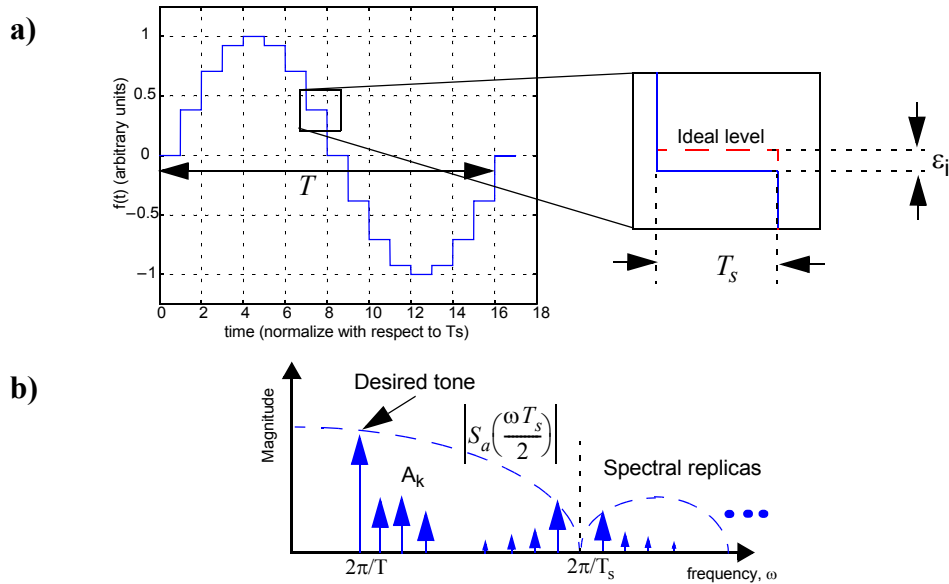
Firstly, let us describe each of the blocks used in the analysis separately, and then we will present the results of combining these blocks.

*Generation of the function  $f(t)$*

Concerning the generation of  $f(t)$ , the objective is to generate a step-wise sinewave with  $N$  steps per period of duration  $T_s$ . A trade-off can be established between the number of step levels composing  $f(t)$  and the selectivity of the filtering stage. A high number of levels will push the spectral replicas of the signal to higher frequencies, which allows to relax the specifications of the filter, but increases the overhead and complexity in the implementation of  $f(t)$ . On the contrary, a low number of step levels reduces this complexity, but the spectral replicas are in this case closer to the main frequency and will need a sharper filter to be attenuated.

On the other hand, in a practical case the step levels will be affected by random variations. These deviations will introduce errors,  $\epsilon_j$ , in the step levels as shown in Figure 2.13. It means that function

FIGURE 2.13. Step-wise sinewave  $f(t)$  including errors in the step levels: a) time domain; b) frequency domain



$f(t)$  will be composed by a main harmonic at frequency  $1/NT_s$ , unwanted harmonics,  $A_k$ , due to the errors at multiples of such frequency,  $k/NT_s$ ,  $k = 2, 3, \dots$ , and replicas of the spectrum around  $m/T_s$ ,  $m=1, 2, \dots$ , modulated by the sampling function  $S_a(\omega T_s/2)$  (see Figure 2.13).

Possible errors in the duration of the steps  $T_s$  can be modeled as an added jitter noise. However, these timing errors have not been included in the presented model for simplicity.

#### *Ideal linear filtering*

Concerning the system transfer function  $H(s)$ , we are going to consider lowpass and bandpass, first and second order filtering sections; the effect of a higher order filter can be straightforward derived from them. First order lowpass and second order lowpass and bandpass systems can be described in terms of their transfer functions as,

$$H_1^{LP}(s) = \frac{k}{1 + s/\omega_0}, \quad (2.7)$$

$$H_2^{LP}(s) = \frac{k\omega_0^2}{s^2 + (\omega_0/Q)s + \omega_0^2}, \quad (2.8)$$

$$H_2^{BP}(s) = \frac{k(\omega_0/Q)s}{s^2 + (\omega_0/Q)s + \omega_0^2}, \quad (2.9)$$

respectively, where  $k$  is a scale factor,  $\omega_0$  is the angular frequency of the pole(s) and  $Q$  is the pole quality factor (assuming complex conjugate poles).

#### *Non-linear behavior*

With respect to the non-linearity of the system, it depends strongly on the particular filtering stage, its architecture and its circuit topology. In general, the non-linear characteristic can be modelled by a polynomial in the form,

$$y(t) \approx x(t) + \lambda_2 x^2(t) + \lambda_3 x^3(t) + \dots \quad (2.10)$$

where  $x(t)$  represents the output of the ideal linear filtering, coefficients  $\lambda_i$  model the non-linearity of the system, and  $y(t)$  is the output of the system. Usually, a third order polynomial is enough for modeling purposes, although higher order polynomials can be also used for strongly non-linear systems.

#### *Analysis results*

Let us consider now the combination of the discussed blocks to model the proposed system and study its performance limitations.

The frequencies of the unwanted harmonics of function  $f(t)$  have to be placed in the rejection band of the system, while the desired tone (its main harmonic) is placed in the passband of the filter, as represented in Figure 2.11. In our particular case in which  $f(t)$  is a  $N$ -step sinewave of duration  $T_s$ , the best choice is clearly to make,

$$\omega_0 = \frac{2\pi}{NT_s} \quad (2.11)$$

because it means that the frequency of the signal will be close to the peak gain of the filter (for  $Q > 1/2$ ) while the harmonics will be in the rejection band. In this way, the filter contributes to attenuate the  $m$ -th harmonic with respect to the main one, in the steady state, by a factor,

$$A_m^{LP1} = \frac{|H_1^{LP}(s)|_{s=jm\omega_0}}{|H_1^{LP}(s)|_{s=j\omega_0}} = \sqrt{\frac{2}{1+m^2}} \quad (2.12)$$

$$A_m^{LP2} = \frac{|H_2^{LP}(s)|_{s=jm\omega_0}}{|H_2^{LP}(s)|_{s=j\omega_0}} = \frac{1/Q}{\sqrt{(1-m^2)^2 + (m/Q)^2}} \quad (2.13)$$

$$A_m^{BP2} = \frac{|H_2^{BP}(s)|_{s=jm\omega_0}}{|H_2^{BP}(s)|_{s=j\omega_0}} = \frac{m/Q}{\sqrt{(1-m^2)^2 + (m/Q)^2}} \quad (2.14)$$

where  $A_m^{LP1}$ ,  $A_m^{LP2}$ , and  $A_m^{BP2}$  represent the cited attenuation in the case of first order lowpass filtering, second order lowpass filtering, and second order bandpass filtering, respectively. Functions in (2.12), (2.13) and (2.14) are represented in Figure 2.14. As it could be anticipated, the first order section gives the poorest attenuation of the unwanted components, while the high- $Q$  second order lowpass section gives the best results in this line.

To estimate the effect of this ideal filtering, a set of Monte Carlo numerical simulations using maximum errors of 0.1% and 1% in the levels of the stepwise sinewave and applied to the filtering sections above (with different  $Q$  values for the case of the second order sections) have been carried out. Figure 2.15 shows the obtained worst cases in terms of Spurious-Free Dynamic Range (SFDR) and Total Harmonic Distortion (THD) for a maximum error in the step levels of 0.1% as a function of the number of step levels and the quality factor  $Q$ . On the other hand, Figure 2.16 shows the worst cases for  $Q = 5$  as a function of the number of step levels and its maximum error.

It is clear to see that for a low number of step levels the obtained THD and SFDR are limited mainly by the first spectral replica, which, in this case, is close to the main tone of  $f(t)$ . This effect can be observed in Figure 2.16, where it is shown that for  $N \leq 16$  there is no significant improvement in the performance when the error level is decreased. From  $N > 16$ , the effect of the replicas can be neglected, as they are far enough from the main tone and are effectively canceled by the filtering. The performance in this case is mainly limited by the accuracy of the steps and the selectivity of the filter.

FIGURE 2.14. Attenuation due to filtering: a) first order lowpass, b) second order lowpass, and c) second order bandpass

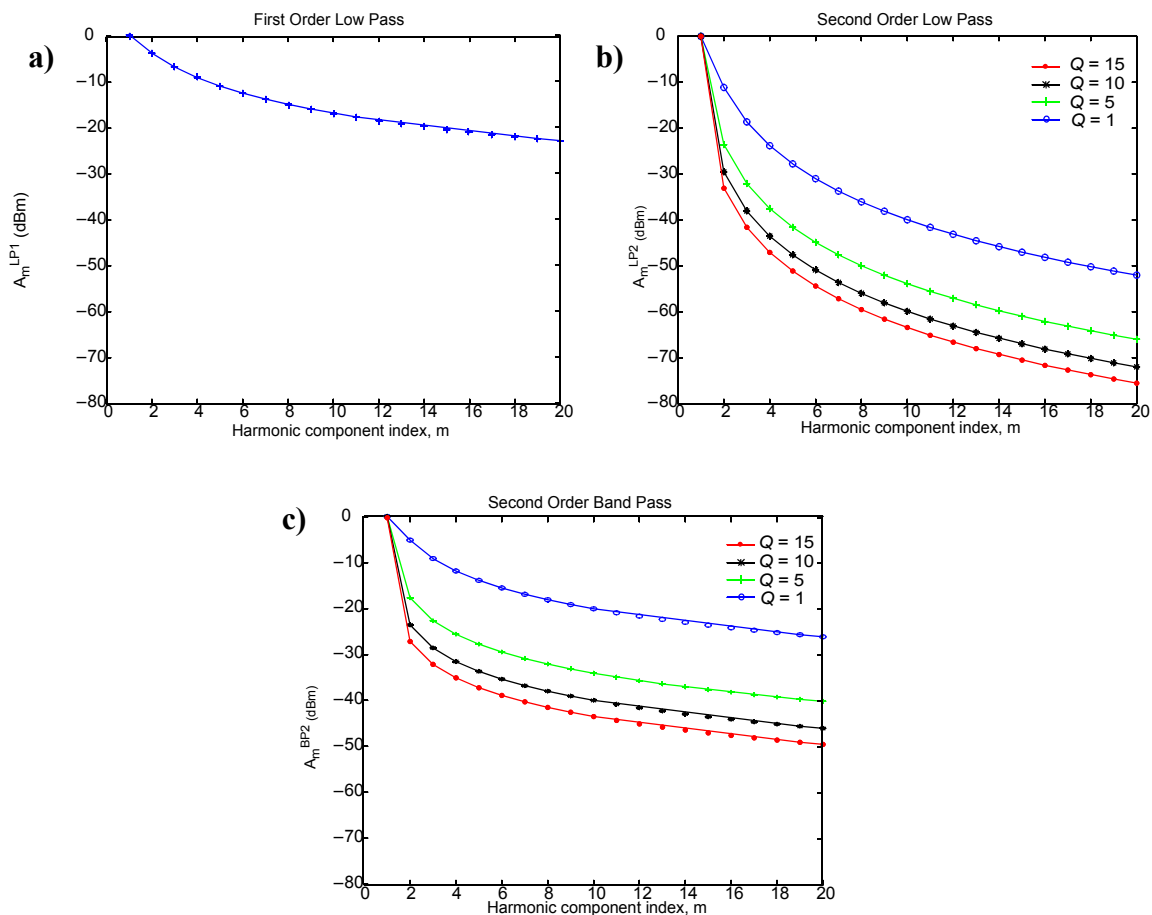
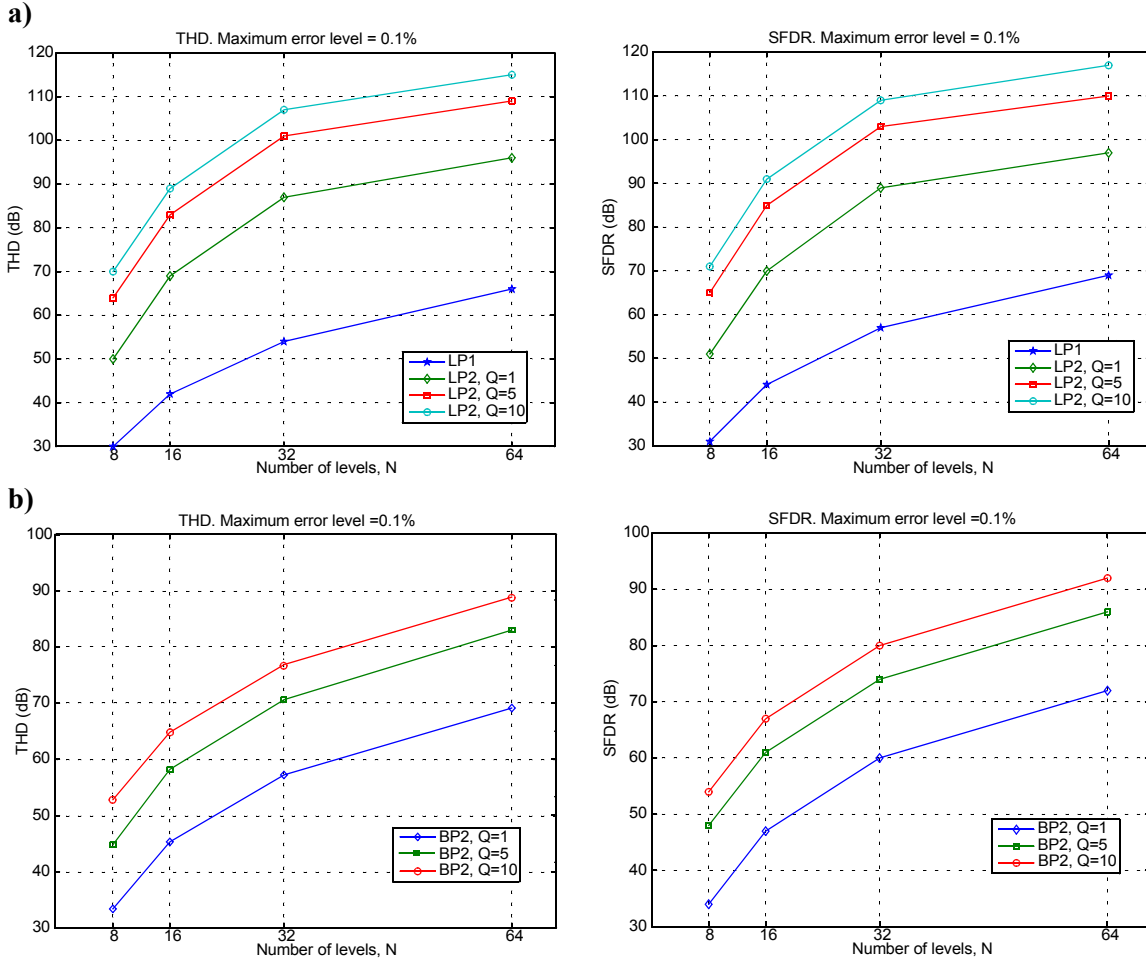
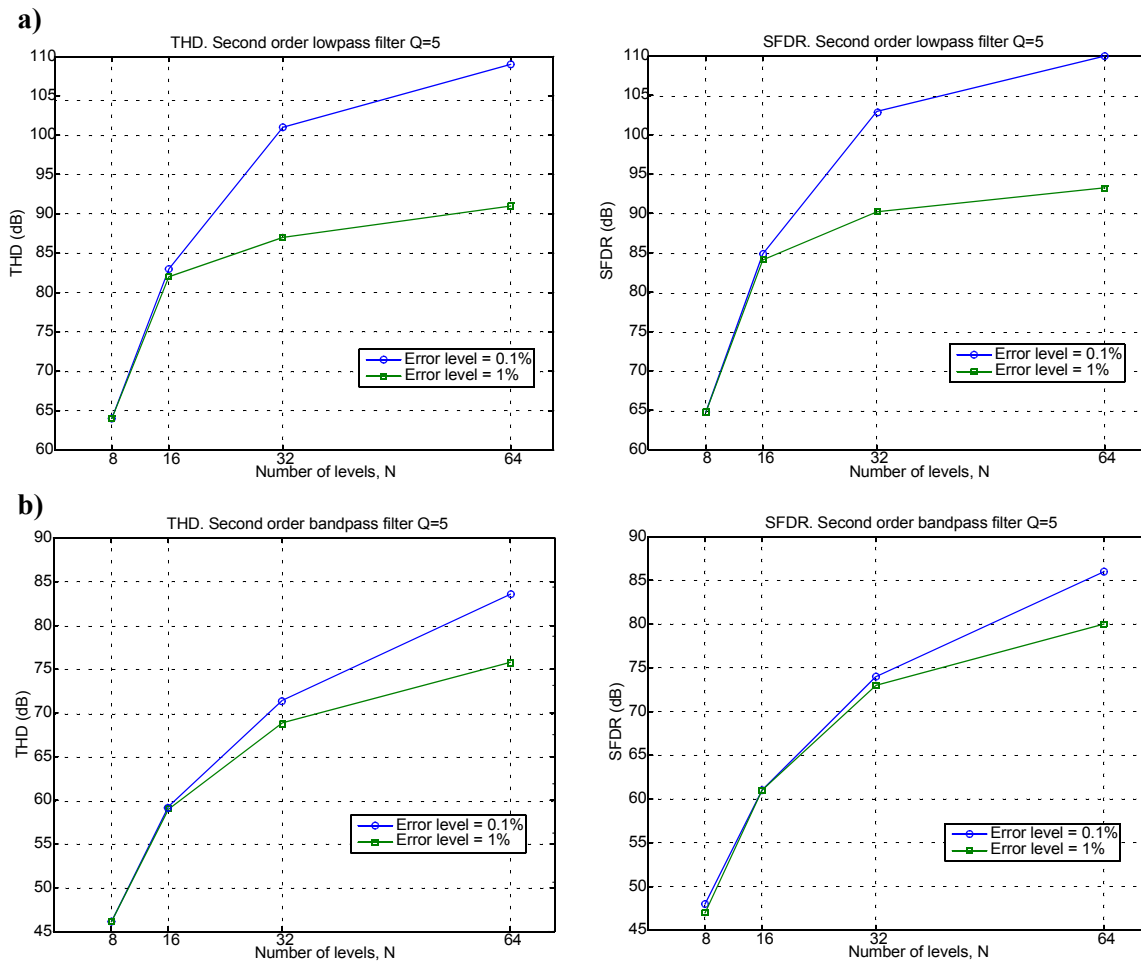


FIGURE 2.15. THD and SFDR estimation for maximum step level error of 0.1% as a function of  $Q$ : a) Lowpass sections; b) Bandpass sections





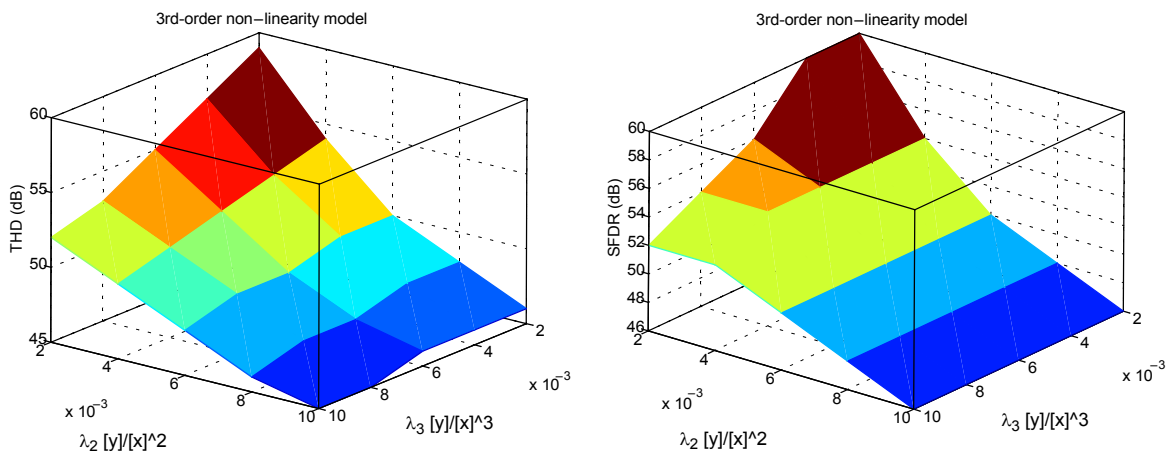
**FIGURE 2.16. THD and SFDR estimation for  $Q = 5$  as a function of the step level error:**  
**a) Second-order lowpass; b) Second-order bandpass**



The obtained results show that a very good SFDR and THD can be theoretically obtained for a relatively low number of steps per period and low order filtering. For example, a SFDR and THD around 80dB are expected for  $N=16$  and  $Q=5$  with an error in the levels of 1% in the case of the 2nd-order lowpass filtering. A comparison can be made with other generation techniques in order to place these results into perspective. For instance, if the memory-based  $\Sigma\Delta$  generation strategy in Figure 2.4c is considered with a 200-bit register and 3rd-order lowpass ideal linear filtering of an optimized 2nd-order  $\Sigma\Delta$ -encoded sequence, the SFDR and THD, obtained by numerical simulation, are approximately 75dB and 72dB, respectively, but worst cases due to very small deviations of the parameters of the analog signal to be coded (such as the phase or the amplitude) may result in a significant drop in the signal quality to below 50dB SFDR and THD [50]. Matching the expected results of the proposed approach with this  $\Sigma\Delta$ -based method demands either a longer register, a higher order filter, or a combination of both. However, it is convenient to remark that these theoretical results are optimistic, since the non-linearity of the filter has not been considered yet, nevertheless this non-linearity will affect equally to both systems if the same output filter is used for both.

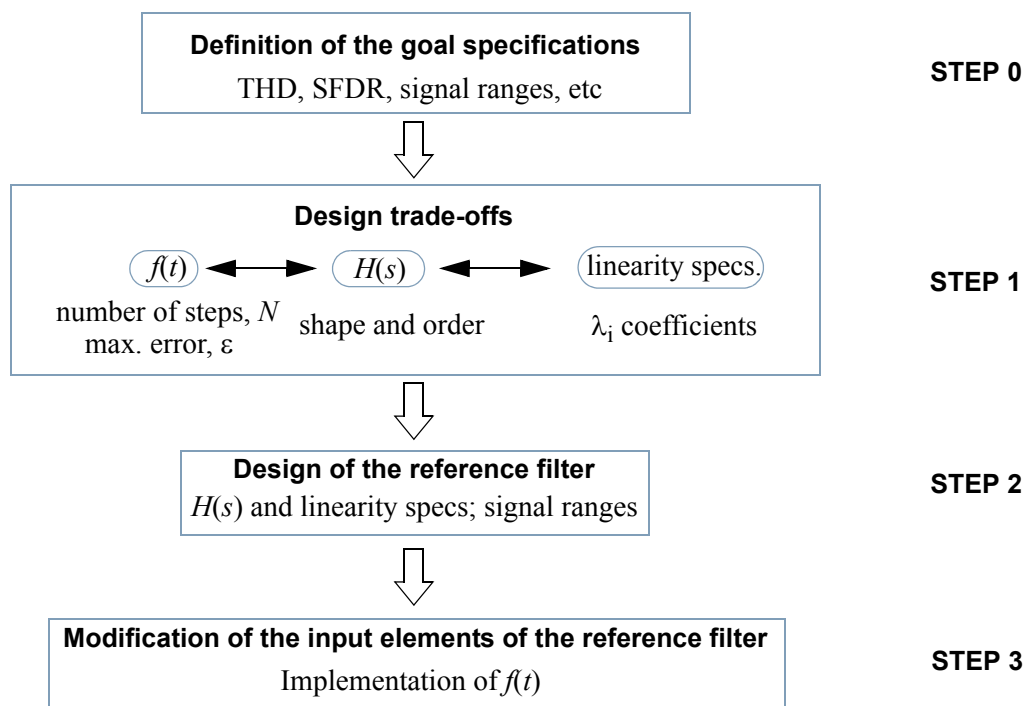
Concerning the non-linearity of the system, it should be clear that it is very specific of each particular implementation of the filtering stage. Nevertheless, the polynomial model (2.10) can be used to give some insight at high level. Figure 2.17 shows the THD and SFDR introduced by (2.10), obtained with a third order model for different values of the coefficients  $\lambda_2$  and  $\lambda_3$  when  $x(t)$  is a unit-amplitude pure sinewave (in arbitrary units). Obviously, minimizing the non-linear coefficients  $\lambda_2$  and  $\lambda_3$  leads to better THD and SFDR figures.

**FIGURE 2.17. THD and SFDR in a third order polynomial model**



The discussed high level model can guide the designer towards the set of specifications for the filter and the  $f(t)$  function in order to implement a generator with a desired performance. In fact, it defines a design methodology, that has been represented in the flow diagram in Figure 2.18. Firstly, the trade-off between the choice of  $f(t)$ ,  $H(s)$ , and the system non-linearity has to be considered to get a set of parameters compatible with the desired generator performance. The high level model discussed in this section is very useful for this purpose. After that, the next step is to propose a particular analog filter architecture compatible with the  $H(s)$  and linearity specifications obtained in the previous step. Once the filtering stage is defined, to complete the design of the generator the input elements of the filter have to be modified to implement the  $f(t)$  function selected in the first step. In fact, the design flow is very similar to the design of an analog filter, except for the modification of the input elements.

FIGURE 2.18. Conceptual design flow for the proposed signal generator



## 2.4. Summary

The generation of high quality analog periodic signals, and particularly, sinewave signals, is one of the key point in many analog and mixed-signal test schemes. Traditional test methods for analog and mixed-signal systems normally use periodic signals as test stimuli and apply complex processing algorithms to the response in order to extract the targeted test parameters. The emulation of these test schemes for on-chip implementations and BIST applications in the analog and mixed-signal domains are normally prohibitive due to the excessive overhead, except in very complex systems where the required hardware is already available on-chip.

This chapter has presented a novel and efficient methodology for analog sinewave generation with reduced circuitry resources. It is based on a modified low-order analog filter with a DC input and programmable input elements, in such a way that the filter itself performs two operations: the signal generation and the filtering of the unwanted components.

The performance limits of the proposed methodology have been theoretically estimated. The performance of the generator is mainly limited by three different factors: the accuracy of the generated step levels (which is related to the matching between the input elements of the filter), the selectivity of the filter, and the non-linear characteristic of the filter itself. These limitations have been discussed, and design guidelines have been given for the implementation of the proposed sinewave generator.

Compared to other approaches previously reported, the proposed solution presents some advantages:

- Reduced circuitry: the required resources are mainly reduced to a filtering stage.
- Good trade-off between signal quality and filter complexity: the use of low order filters produces results that are comparable to other strategies that employ high-order filtering.

On the other hand, the presented generator contains the main attributes for BIST solutions: digital programming and control capability, robustness, low area overhead, and low design effort.

## Practical Design of Analog Sinewave Generators and Experimental Results

*This chapter presents two prototypes of the analog sinewave signal generator described in the previous chapter: a continuous-time generator and a discrete-time one, along with a detailed description of the design methodology. The developed demonstrators have been integrated in a standard CMOS 0.35 $\mu\text{m}$  technology. Experimental measurements in the lab verify the feasibility of the approach and the functionality of the developed prototypes.*

### 3.1. Introduction

In this chapter two different integrated prototypes have been developed as a vehicle to illustrate the design methodology and the feasibility of the presented generator, using a standard  $0.35\mu\text{m}$  CMOS technology. We are going to detail the design of the proposed generation scheme in two of the most representative filter design styles: OTA-C filters in the continuous-time domain, and SC filters in the discrete case.

The design methodology that is going to be followed was presented in the previous chapter, and can be divided into three main stages:

- Firstly, the trade-off between the choice of the periodic function  $f(t)$  and the filtering stage has to be considered.
- After that, a particular filter architecture compatible with the desired performance is proposed.
- Finally, once the design of the filter is completed its input elements are modified to implement the selected  $f(t)$  function.

In the following, the design of the continuous-time OTA-C and discrete-time SC generators will be considered separately. Section 3.2 details the design of the OTA-C case, while Section 3.3 discusses the SC one. Section 3.4 summarizes experimental results obtained from the prototypes, and finally Section 3.5 remarks the key points of the chapter.

### 3.2. OTA-C prototype

This section explains the development of a continuous-time sinewave generator using the OTA-C technique in a standard  $0.35\mu\text{m}$ -3.3V CMOS technology. The general set of goal specifications, which are listed in Table 3.1, corresponds to typical performance parameters of OTA-C filters in the said technology.

**TABLE 3.1. Goal specifications for the OTA-C generator prototype**

Parameter	Value
Frequency range	from 20MHz to 40MHz
Amplitude range	up to 250mV peak-to-peak
Linearity	better than 50dB THD and SFDR in the desired frequency and amplitude range

The next subsections detail the design of the OTA-C generator following a top-down methodology.

### 3.2.1. General considerations

The first step in the design of the generator is to define the characteristics of the function  $f(t)$  and the filtering stage compatible with the desired specifications. In the view of the performance analysis detailed in the previous chapter, the combination of a 16-step sinewave as  $f(t)$  and a second-order lowpass filtering stage with a relatively low quality factor  $Q$  around  $Q=5$ , gives THD and SFDR figures above the desired specifications, while represents a good trade-off solution between performance and design complexity. This is illustrated in Figure 2.16 which is reproduced here in Figure 3.1 for convenience. It is interesting to notice that using only 8 step levels may be also a viable solution. However, our choice of 16 levels pushes the spectral replicas to higher frequencies and gives a conservative margin over the goal specifications in terms of linearity.

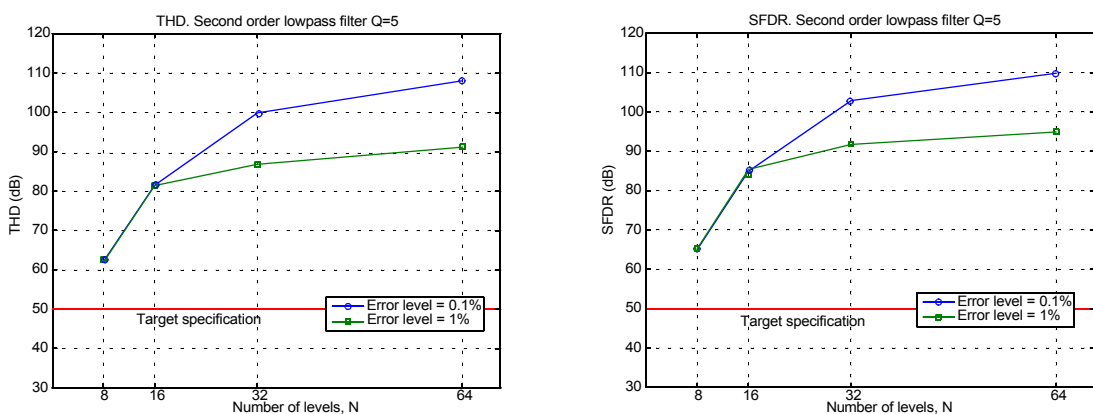
Thus, function  $f(t)$  will be a step-wise sinewave of period  $T$  with 16 levels of duration  $T_s=T/16$ . That is,  $f(t)$  can be expressed in the interval  $[0,T)$  as,

$$f(t) = \sin\left(\frac{k\pi}{8}\right) \quad \frac{kT}{16} < t < \frac{(k+1)T}{16} \quad (3.1)$$

$$k = 0, 1, \dots, 15$$

The symmetry of the selected 16-step sinewave makes necessary only 5 values to describe the full waveform, and its spectral replicas will be conveniently far from the main tone, which makes it easy to place them in the rejection band of the second-order filter while keeping the main tone in the

**FIGURE 3.1. THD and SFDR estimation as a function of the number of step levels**



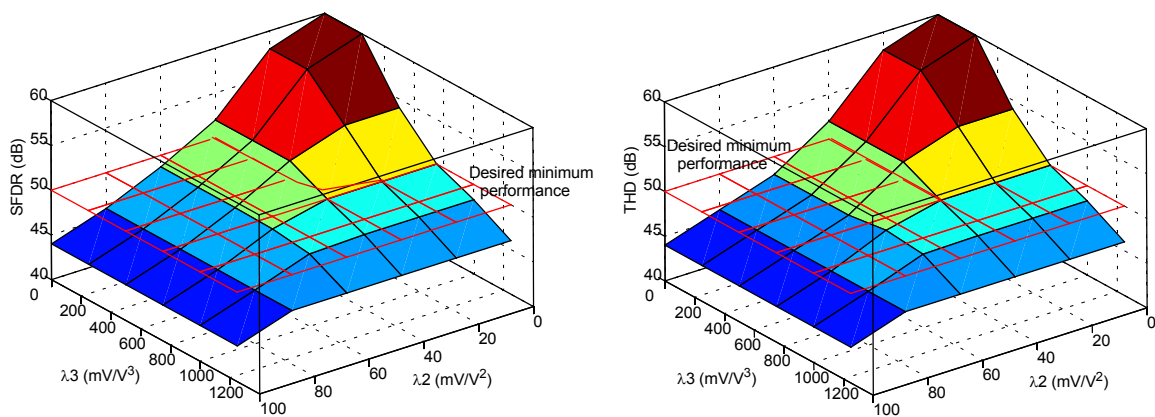
passband. To improve the rejection of the non-desired frequency components, the frequency of the generated signal will be placed at the filter peak frequency. That is, if  $\omega_0$  is the central frequency of the filter, then making,

$$\omega_0 = \frac{2\pi}{T} = \frac{2\pi}{16T_s} \quad (3.2)$$

will assure that the non-desired components lie inside the rejection band.

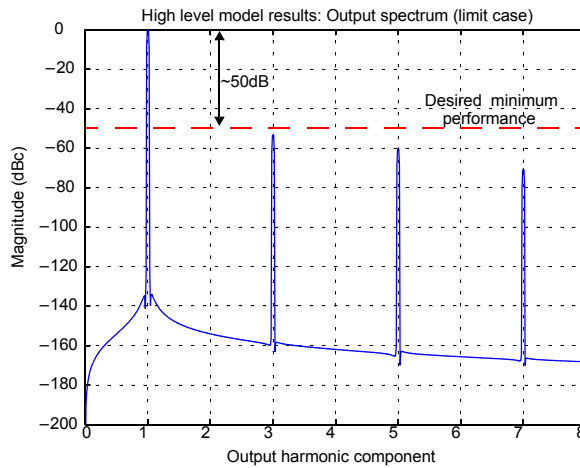
Concerning the linearity of the filtering stage, assuming a third-order polynomial model with the notation introduced in the previous chapter, Figure 3.2 shows an exploration of the design space in terms of the non-linear coefficients  $\lambda_2$  and  $\lambda_3$ . In the view of this exploration, and assuming that coefficient  $\lambda_2$  can be made close to zero using a fully-differential architecture, the third-order coefficient  $\lambda_3$  has to be lower than  $750\text{mV/V}^3$  in the defined signal range in order to fulfill the desired linearity specifications in Table 3.1. Under these circumstances, using the proposed high level model, it can be determined that the step-levels of function  $f(t)$  can be affected by deviations up to 10% of its intended value without degrading the linearity of the generated signal. Although this deviation range may seem relatively high, it is coherent with the previous design choices: the linearity of the generator is mainly determined by the linearity of the filter core, and in a lesser extent by the first spectral replica, so the errors in the step levels have little impact in the performance. Figure 3.3 shows the spectrum of the generator output obtained with the high level model under the discussed limit conditions of error level and linearity. The obtained result agrees with the minimum goal performance.

**FIGURE 3.2. SFDR and THD estimations using a third-order model for a 250mVpp signal. The plane at 50dB marks the desired minimum performance.**





**FIGURE 3.3. Output spectrum obtained with the high level model for the limit case ( $N=16$ , error level=10%,  $\lambda_2=0$ ,  $\lambda_3=750\text{mV/V}^3$ , peak-to-peak output voltage=250mV)**



**FIGURE 3.4. General block diagram of the OTA-C generation scheme**

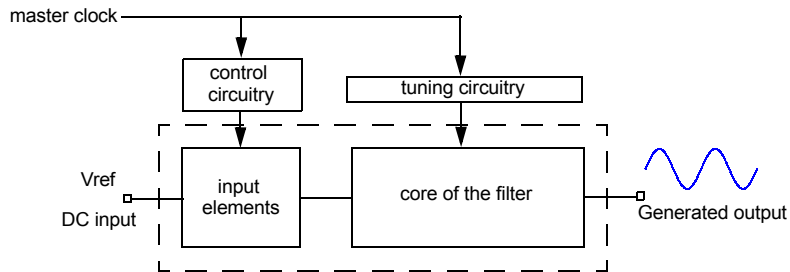
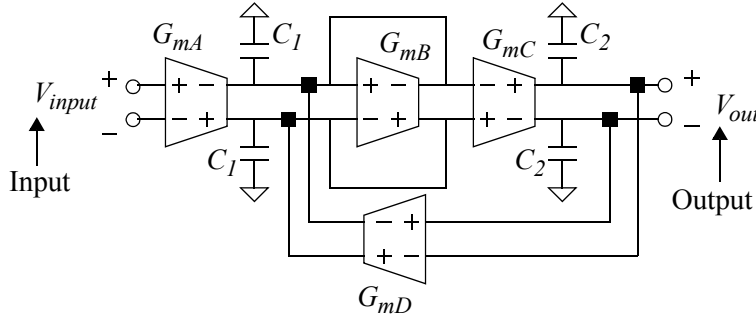


Figure 3.4 shows a general block diagram of the OTA-C generator architecture. It consists of the selected second-order lowpass filter, whose input devices have been modified to generate the step-levels of a 16-step sinewave. The amplitude of the generated signal is controlled by the input DC level, labelled  $V_{ref}$  in Figure 3.4, that, as stated by equation (2.5), acts as an output scaling factor. The programming of the signal frequency is achieved by tracking the frequency of the generated signal to the central frequency of the filter according to equation (3.2). This can be easily done by the frequency tuning of the filter. The central frequency is an integer division of the master clock frequency of the tuning circuitry. The tracking in (3.2) can be achieved by clocking the input elements with the adequate division of the master clock. However, in this first prototype the necessary tuning control will be provided externally.

FIGURE 3.5. Basic block diagram of the OTA-C reference filter



### 3.2.2. System level

Let us discuss separately the design of the reference second-order filtering stage, and after that, we will introduce the modification of its input elements to build the desired generator.

#### A. Reference filter

The selected filter block diagram is shown in Figure 3.5. It is a typical fully-differential second-order lowpass OTA-C implementation. The transfer function of the filter,  $V_{out}/V_{input}$  in the Laplace domain can be easily obtained by simple analysis,

$$H(s) = \frac{4 \frac{G_{mA} G_{mC}}{C_1 C_2}}{s^2 + s \frac{2G_{mB}}{C_1} + 4 \frac{G_{mC} G_{mD}}{C_1 C_2}} = \frac{k\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2} \quad (3.3)$$

where the scaling factor  $k$ , the pole quality factor  $Q$ , and the central frequency  $\omega_0$ , are given by,

$$k = \frac{G_{mA}}{G_{mD}} \quad (3.4)$$

$$Q = \frac{C_1}{G_{mB}} \sqrt{\frac{G_{mC} G_{mD}}{C_1 C_2}} \quad (3.5)$$

$$\omega_0 = \sqrt{4 \frac{G_{mC} G_{mD}}{C_1 C_2}} \quad (3.6)$$

Taking into account the desired generator specifications, Table 3.2 shows a set of design parameters compatible with these choices. The transconductor values shown in Table 3.2 correspond to the needed transconductor tuning range to achieve the extreme frequency range values 20MHz and 40MHz approximately. The pole quality factor is set to 5, and the scaling factor to 1, in order to achieve a moderate peak gain ( $\sim kQ$ ) of 14dB.

**TABLE 3.2. Design parameters in Figure 3.5 (tuning range for central frequency from 20MHz to 40MHz)**

$G_{mA}$	275 $\mu$ A/V to 550 $\mu$ A/V	$G_{mD}$	275 $\mu$ A/V to 550 $\mu$ A/V
$G_{mB}$	55 $\mu$ A/V to 110 $\mu$ A/V	$C_1$	4 pF
$G_{mC}$	275 $\mu$ A/V to 550 $\mu$ A/V	$C_2$	4 pF

The design parameters have been chosen using matching considerations. Thus, capacitors have been made equal, and transconductors are integer multiples of a unit transconductor. That is, transconductors  $G_{mA}$ ,  $G_{mC}$ , and  $G_{mD}$  have been chosen to be five times larger than the unit transconductor  $G_{mB}$ , and can be built from five matched unit transconductors  $G_{mB}$  in parallel.

Concerning the linearity specifications, the non-linear characteristic of a fully-differential transconductor can be approximated by a third order polynomial in the form,

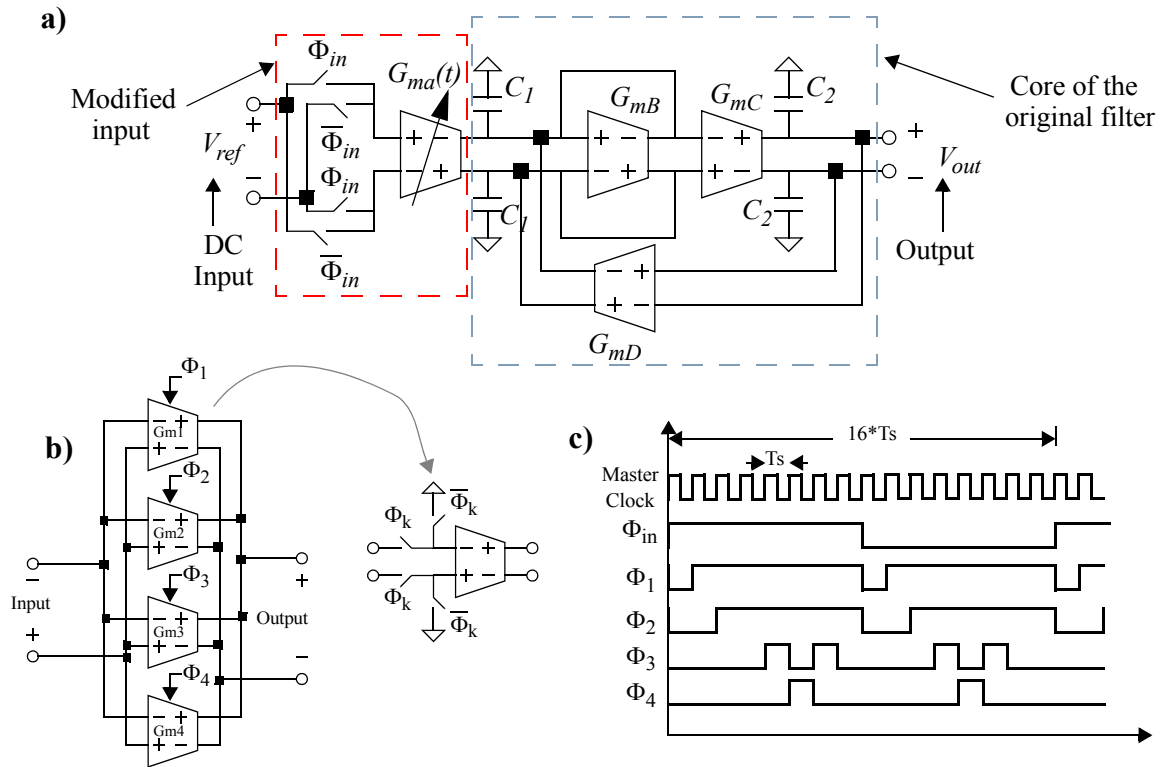
$$I_{out} \approx G_m V_{in} + \alpha_3 V_{in}^3 \quad (3.7)$$

where  $I_{out}$  is the output current of the transconductor,  $V_{in}$  is its input voltage,  $G_m$  is its linear transconductance, and  $\alpha_3$  is a third-order non-linear coefficient. To assure that the goal linearity specifications are fulfilled, high level simulations of the whole filter were performed sweeping the  $\alpha_3$  coefficient. According to the obtained results, the non-linear coefficient  $\alpha_3$  of the unit transconductor has to be kept below 50 $\mu$ A/V<sup>3</sup> in the selected signal range.

### B. OTA-C sinewave generator

Following the proposed design methodology, the next step in the design flow is to modify the input elements of the developed OTA-C reference filter to transform it into the desired OTA-C sinewave generator. The system level block diagram of the developed generator is shown in Figure 3.6a. The only modification with respect to the reference filter is that the input transconductor  $G_{mA}$  has been replaced by a switching scheme controlled by the digital signal  $\Phi_{in}$  and a programmable transconductor  $G_{mA}(t)$  to implement the step-wise sinewave levels. Transconductor

FIGURE 3.6. a) Block diagram of the OTA-C sinewave generator. b) Time-variant transconductor implementation. c) Time scheme



$G_{ma}(t)$  is composed by four transconductors in parallel ( $G_{m1}$  to  $G_{m4}$ ) as depicted in Figure 3.6b, whose contributions are switched on or off in an incremental way accordingly to the time scheme shown in Figure 3.6c (Appendix 1 details a proposal for the generation of these programming signals). In this way, the required 5 steps of the positive half sinewave are generated, while the input switching scheme controlled by signal  $\Phi_{in}$  sets the weight, positive or negative, of the step. The resulting transconductance  $G_{ma}(t)$  can be described as,

$$G_{ma}(t) = \{ \Phi_{in}(t) - \overline{\Phi_{in}(t)} \} \left\{ \sum_{k=0}^4 \Phi_k(t) G_{mk} \right\} \quad (3.8)$$

where  $G_{m0} = 0$ , and  $G_{mk}$  for  $k=1, \dots, 4$  are given by,

$$G_{mk} = G_{mA} \left[ \sin\left(\frac{k\pi}{8}\right) - \sin\left(\frac{(k-1)\pi}{8}\right) \right] \quad k = 1, 2, 3$$

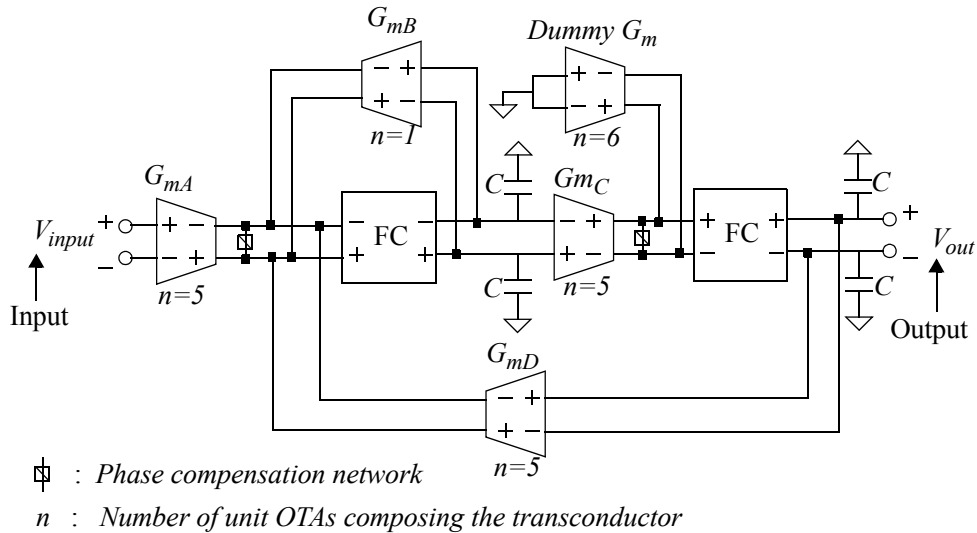
$$G_{m4} = G_{mA} \left[ \sin\left(\frac{4\pi}{8}\right) - \sin\left(\frac{2\pi}{8}\right) \right] \quad k = 4$$
(3.9)

The possible errors in the step levels defined by  $G_{ma}(t)$  are due to two main factors: the possible mismatching between transconductors, which may shift the transconductance of the steps, and the offset of each elemental transconductor  $G_{mk}$ , which adds to the output current of the programmable transconductor. These deviations will be estimated in the next section.

### C. Practical implementation

The basic block diagram in Figure 3.5 has to be modified for its practical realization. Folded-cascode stages are used to increase the output impedance of the transconductors, and they are shared by all the transconductors that are incident in the same node. In addition, dummy transconductors are added to the input nodes of the folded-cascode elements to ensure that all these nodes have the same parasitic capacitance associated with them. These dummy transconductors consist of a transconductor whose input nodes have been shorted to analog ground. Phase compensation

**FIGURE 3.7. The complete block diagram including dummy elements, the folded-cascode stages, and the phase compensation networks**



networks are also included in the design to minimize the excess phase in the integrators. Given that the introduced dummy capacitors assure that the parasitic capacitance at the input of each folded-cascode stage is the same, then all the integrators of the filter will have the same excess phase and, therefore, the same phase compensation network can be used to minimize the phase error of the integrators. Figure 3.7 shows the block diagram of the OTA-C second-order lowpass filter including the said folded-cascode stages, dummy transconductors, and phase compensation networks.

### 3.2.3. Schematic level: building blocks design

#### *Unit transconductor*

Multiple OTA architectures have been proposed in the literature [59]-[63]. In our design, we are going to use the linearized OTA structure presented in [59] due to its simplicity and its good linearity properties. Figure 3.8 shows the transistor level schematic of the adopted unit transconductor and its bias circuitry. It is a typical linearized transconductance structure with a source degeneration resistor (implemented by transistors M2a and M2b in Figure 3.8). The sizes of the transistors in Figure 3.8 are listed in Table 3.3.

**TABLE 3.3. Transistor sizes for the unit OTA**

	<b>M1</b>	<b>M2</b>	<b>M3</b>	<b>M4</b>
<b><math>W/L</math> (<math>\mu\text{m}/\mu\text{m}</math>)</b>	25/0.5	4/0.5	50/1	16/1

Figure 3.9 shows the  $I_{out}$  versus  $V_{in}$  transfer characteristic of the unit transconductor obtained by electrical simulation for  $V_{DD}=3.3\text{V}$  and different bias current conditions. As it is shown, the transconductance value of the unit OTA can be tuned by varying the bias current. The achieved values are between  $G_m=50\mu\text{A}/\text{V}$  for  $I_B=30\mu\text{A}$ , and  $G_m=145\mu\text{A}/\text{V}$  for  $I_B=200\mu\text{A}$ , which exceed the required tuning range defined in Table 3.2.

The linearity of the unit transconductor have been evaluated by adjusting the obtained characteristics using a least-square analysis to the model in (3.7). Restricting the analysis to the linear range of the characteristics (about  $\pm 500\text{mV}$ ) the obtained non-linear coefficient  $\alpha_3$  keeps between  $\alpha_3=7.3\mu\text{A}/\text{V}^3$  for  $I_B=200\mu\text{A}$ , and  $\alpha_3=40\mu\text{A}/\text{V}^3$  for  $I_B=30\mu\text{A}$ , which is in agreement with the linearity requirements. However, it is important to notice that this coefficient can be increased by the contribution of folded-cascode stage.

FIGURE 3.8. Transistor level schematic of the unit OTA

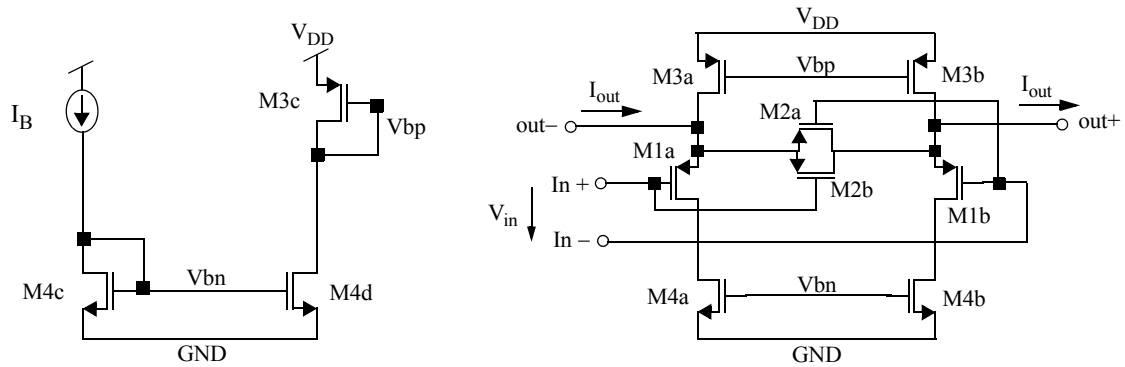
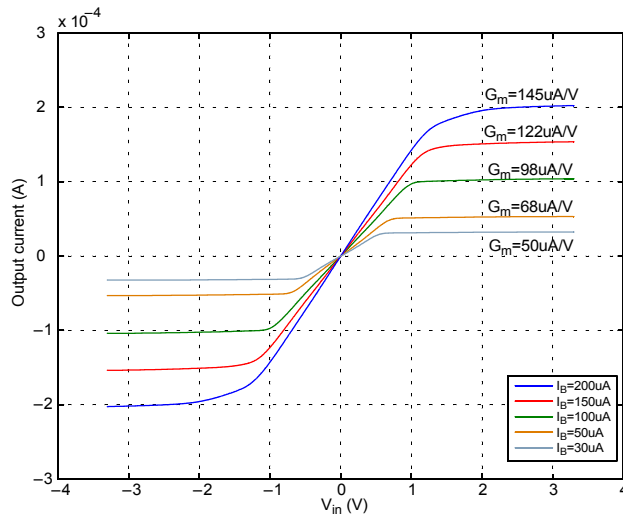


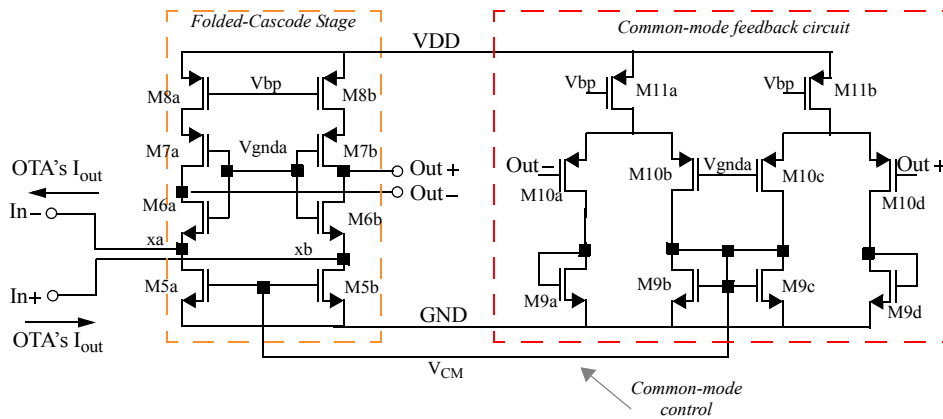
FIGURE 3.9. Transfer characteristic of the unit OTA



*Folded-cascode stage*

Real transconductor elements have a finite output impedance. This output impedance will modify the transfer function of the two integrators composing the reference filter introducing a low-frequency pole [57]. As addressed before, the purpose of introducing the folded-cascode structure is to increase the output impedance of the transconductor. This is done in order to shift the low-frequency pole of the integrators to much lower frequencies, where it cannot do any harm to the filter transfer function.

FIGURE 3.10. Transistor level schematic of the implemented folded-cascode stage



The transistor level schematic of the folded-cascode element is shown in Figure 3.10, together with the necessary common mode feedback circuitry (the bias circuitry is not shown for simplicity). The common mode feedback circuit senses the common mode output voltage and returns a signal through the bias line labelled  $V_{CM}$  to stabilize the common mode output voltage to analog ground [64]. The sizes of the transistors are listed in Table 3.4.

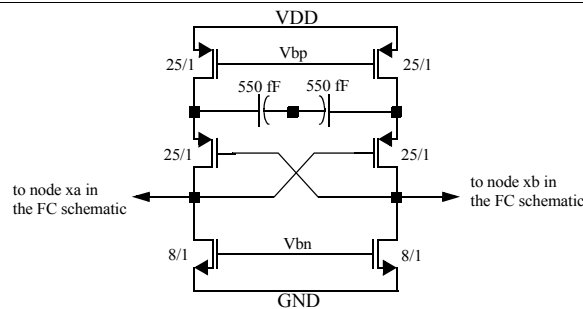
TABLE 3.4. Transistor sizes for the folded-cascode stage and common mode feedback circuit

	<b>M5</b>	<b>M6</b>	<b>M7</b>	<b>M8</b>
<b>W/L (<math>\mu\text{m}/\mu\text{m}</math>)</b>	16/1	16/1	50/1	50/1
	<b>M9</b>	<b>M10</b>	<b>M11</b>	
<b>W/L (<math>\mu\text{m}/\mu\text{m}</math>)</b>	8/1	12/0.5	50/1	

The effect of this stage over the linearity of the unit transconductor has been estimated using a least-square analysis to adjust the  $I_{out}-V_{in}$  characteristic of the full elemental transconductor (composed by the unit OTA plus the folded-cascode stage) to the polynomial model in (3.7). In the linear range of the characteristics (around  $\pm 500\text{mV}$ ) the obtained non-linear coefficient  $\alpha_3$  keeps between  $\alpha_3=13\mu\text{A}/\text{V}^3$  for the transconductance value  $G_m=145\mu\text{A}/\text{V}$ , and  $\alpha_3=45\mu\text{A}/\text{V}^3$  for the case  $G_m=50\mu\text{A}/\text{V}$ , which meets the linearity specifications in the desired signal range.



FIGURE 3.11. Phase compensation network



*Phase compensation network*

Although the increased output impedance provided by the folded-cascode stage moves the previously mentioned low-frequency pole far from the passband edge frequency, the parasitic capacitance at nodes labelled xa and xb in Figure 3.10 creates a high-frequency parasitic pole [57]. This pole modifies the transfer function of the filter near the passband edge frequency. One of the options to deal with this high-frequency parasitic pole is to include a phase compensation network [65] that cancels, at some extent, the contribution of the said parasitic capacitance. Figure 3.11 shows the introduced phase compensation network. As advanced before, dummy transconductors have been introduced (see the general block diagram of the filter in Figure 3.7) to assure that the parasitic capacitance at the input of each folded-cascode stage is the same. Thus, both integrators in the filter have the same parasitic capacitance at nodes xa and xb, and therefore, the same phase compensation network can be used for both integrators.

*Programmable input transconductor*

Concerning the design of the programmable input OTA, the elemental transconductors  $G_{m1}$  to  $G_{m4}$  are similar to the unit transconductor in Figure 3.8, but their input transistors M1 and M2 have been scaled to achieve the transconductance values defined in equation (3.9). Table 3.5 lists the values of the input transistors for each elemental transconductor  $G_{mk}$ .

TABLE 3.5. Size of the input transistors for OTAs  $G_{m1}$  to  $G_{m4}$

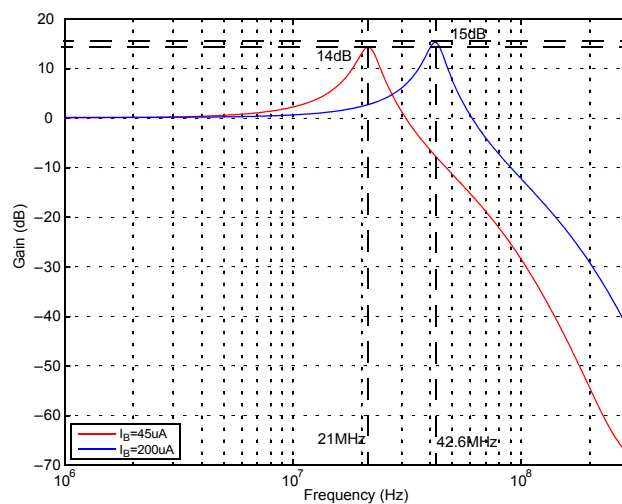
	$G_{m1}$		$G_{m2}$		$G_{m3}$		$G_{m4}$	
	M1	M2	M1	M2	M1	M2	M1	M2
$W(\mu\text{m})$	18	3	69	11.5	28.65	4.75	56	9.35
$L(\mu\text{m})$	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5

Monte Carlo electrical simulations were performed to estimate the possible variations in the transconductance step values of the time-variant transconductor in Figure 3.6b. These simulations include the effects of mismatching between devices and offset of the elemental transconductors. The obtained results show that worst cases will suffer deviations in the step levels below 5% of their intended value. A better matching can be obtained using larger dimensions for the transistors in the input programmable transconductor. However, in this particular case, as stated by the high-level modelling of the system, the generator is insensitive to step error levels up to 10% because the contribution of the non-linearity of the system will mask their effect. Redesigning the input transconductor to achieve a better matching is then not necessary, given that it will not bring an improvement of the system performance.

*Complete filter: electrical simulation results at schematic level*

Once the design of the building blocks is completed, an electrical simulation of the whole filter is performed to check the fulfillment of the target specifications. For this purpose, control signals  $\phi_{in}$ ,  $\phi_1$ ,  $\phi_2$ , and  $\phi_4$  are set to a logic '1' while  $\phi_3$  is set to a logic '0'. It is trivial to verify that in this configuration the system is equivalent to the reference filter previously discussed. The results of the simulations for the two extreme values of the tuning range are registered in Table 3.6, and the magnitude response of the filter is shown in Figure 3.12 for both cases. The obtained performance meets the expected specifications.

**FIGURE 3.12. Magnitude response of the reference filter**



**TABLE 3.6. Performance parameters of the reference filter**

Bias conditions	$V_{DD}=3.3V; I_B=200\mu A$	$V_{DD}=3.3V; I_B=45\mu A$
DC-gain	0dB	0dB
Peak frequency	42.6MHz	21MHz
Peak gain	15dB	14dB
THD @ peak frequency; 250mVpp	67dB	51dB
SFDR @ peak frequency; 250mVpp	67dB	51dB

### 3.2.4. Layout level and post-layout simulations

The OTA-C generator prototype has been laid out following the recommended guidelines for mixed-signal circuits. Purely analog parts are separated from mixed-signal and digital parts by the capacitor array. Also, an output differential buffer has been added at the output of the filter to isolate the output nodes from the parasitic capacitance associated to the output pads. This output buffer is described in Appendix 2. Figure 3.13 shows a diagram of the design floor-planning together with the layout of the system. The core area is  $395\mu m \times 230\mu m$ .

Post-layout simulations of the extracted view were performed. Firstly, the system was simulated when configured as the reference filter to check the specifications of the filtering core of the system. Again, for this purpose, control signals  $\phi_{in}$ ,  $\phi_1$ ,  $\phi_2$ , and  $\phi_4$  are set to a logic ‘1’ while  $\phi_3$  is set to a logic ‘0’. Table 3.7 shows the obtained performance parameters, while Figure 3.14 shows the magnitude response of the filter.

**FIGURE 3.13. Floor-planning and layout of the continuous-time OTA-C sinewave generator**

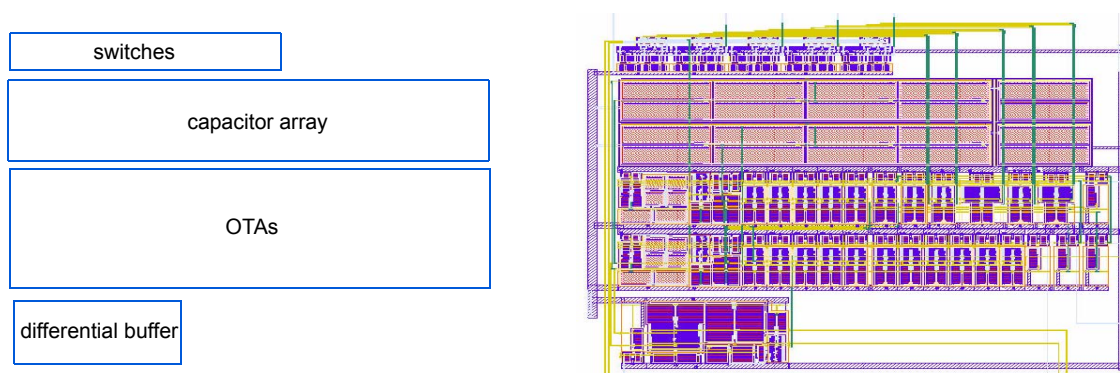
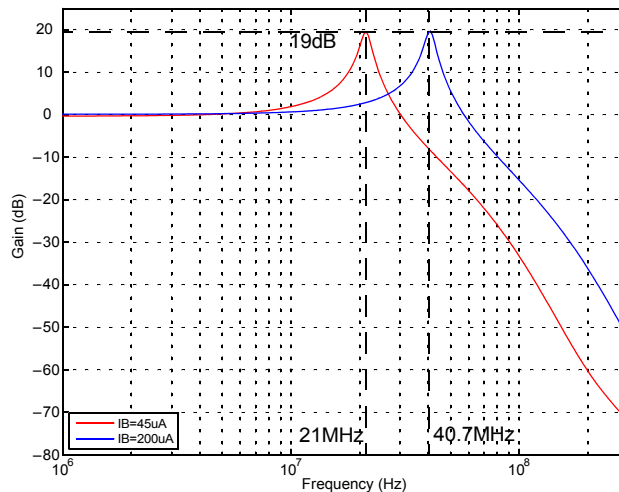


TABLE 3.7. Performance parameters of the system when configured as the reference filter

Bias conditions	$V_{DD}=3.3V; I_B=200\mu A$	$V_{DD}=3.3V; I_B=45\mu A$
DC-gain	0dB	0dB
Peak frequency	40.7MHz	21MHz
Peak gain	19dB	19dB
THD @ peak frequency; 250mVpp	65dB	51dB
SFDR @ peak frequency; 250mVpp	66dB	51dB

FIGURE 3.14. Magnitude response of the system when configured as the reference filter



Due to the contribution of parasitics, the central frequency of the filter is slightly lower compared to the simulation of the filter schematic in the same bias conditions, but still meets the desired specifications. The linearity performance is approximately the same. However, there is a troublesome effect in the increase of the peak gain to 19dB. This increase corresponds to a  $Q$ -enhancement effect ( $Q$  factor rises to 9.8) mainly due to the contribution of parasitics to the previously mentioned high-frequency pole of the integrators composing the filter [66]. This effect may be disadvantageous because, on the one hand, a very high peak gain means that low signal levels have to be maintained at the input to assure that the linear range of the transconductor is not exceeded, and on the other hand, it also increases the noise levels. Since this is just a demonstrator prototype, it is not necessary to redesign and we will simply redefine our peak gain specifications.

Once the performance of the filter core has been checked, the sinewave generator is simulated. Figure 3.15 shows four output waveforms and their spectra, obtained by electrical simulations of the generator extracted view. In these simulations the frequency of the generated signal has been set to 40.7MHz, while its peak-to-peak amplitude has been swept from 175mV to 590mV. In terms of spectral purity, the achieved THD and SFDR keep approximately between 70dB for the 175mVpp signal, and 56dB for the 590mVpp one. It is also clear in Figure 3.15 that the spectral replicas in the  $f(t)$  spectrum are attenuated by the filtering. Another set of simulations is shown in Figure 3.16. This figure shows the obtained linearity parameters when sweeping both the amplitude and the frequency of the generated signal. The achieved performance parameters are listed in Table 3.8.

**FIGURE 3.15. Generator output signal: waveforms and spectra**

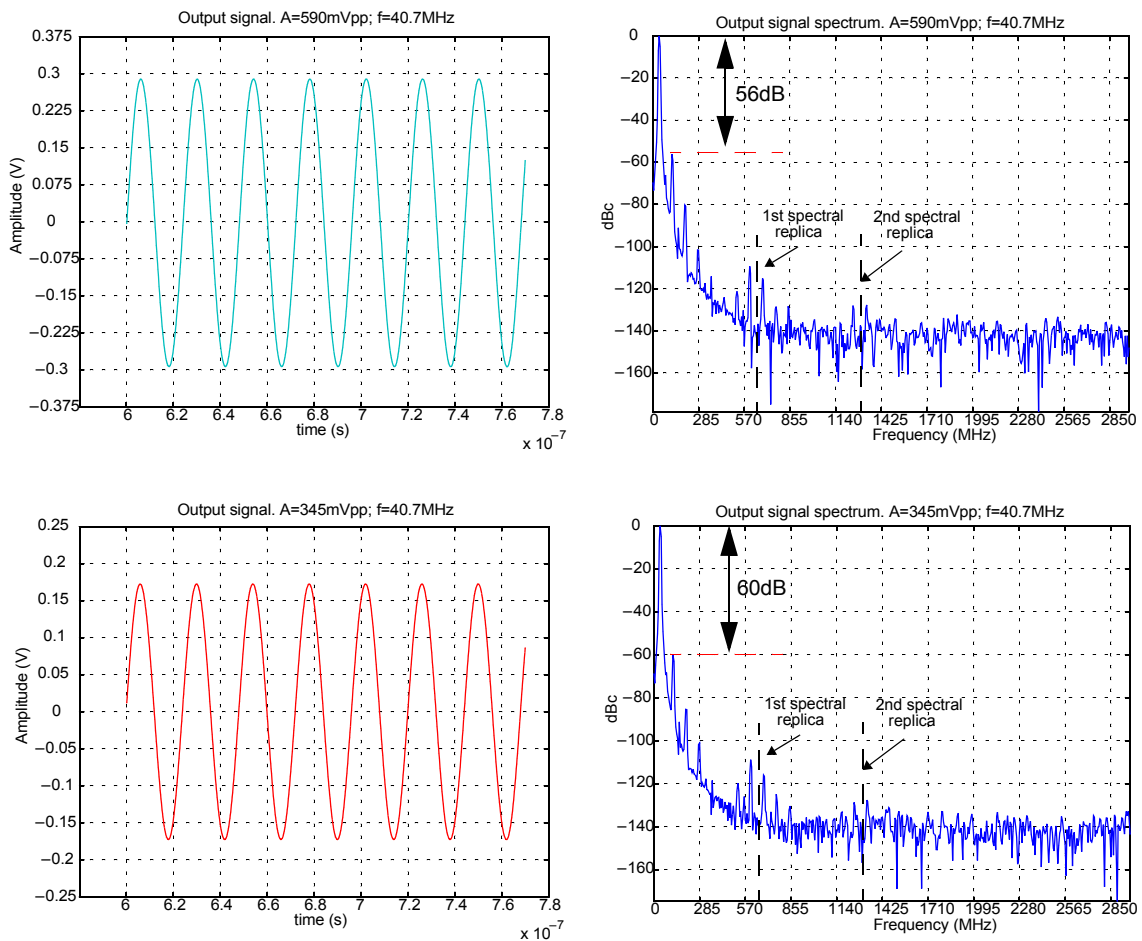
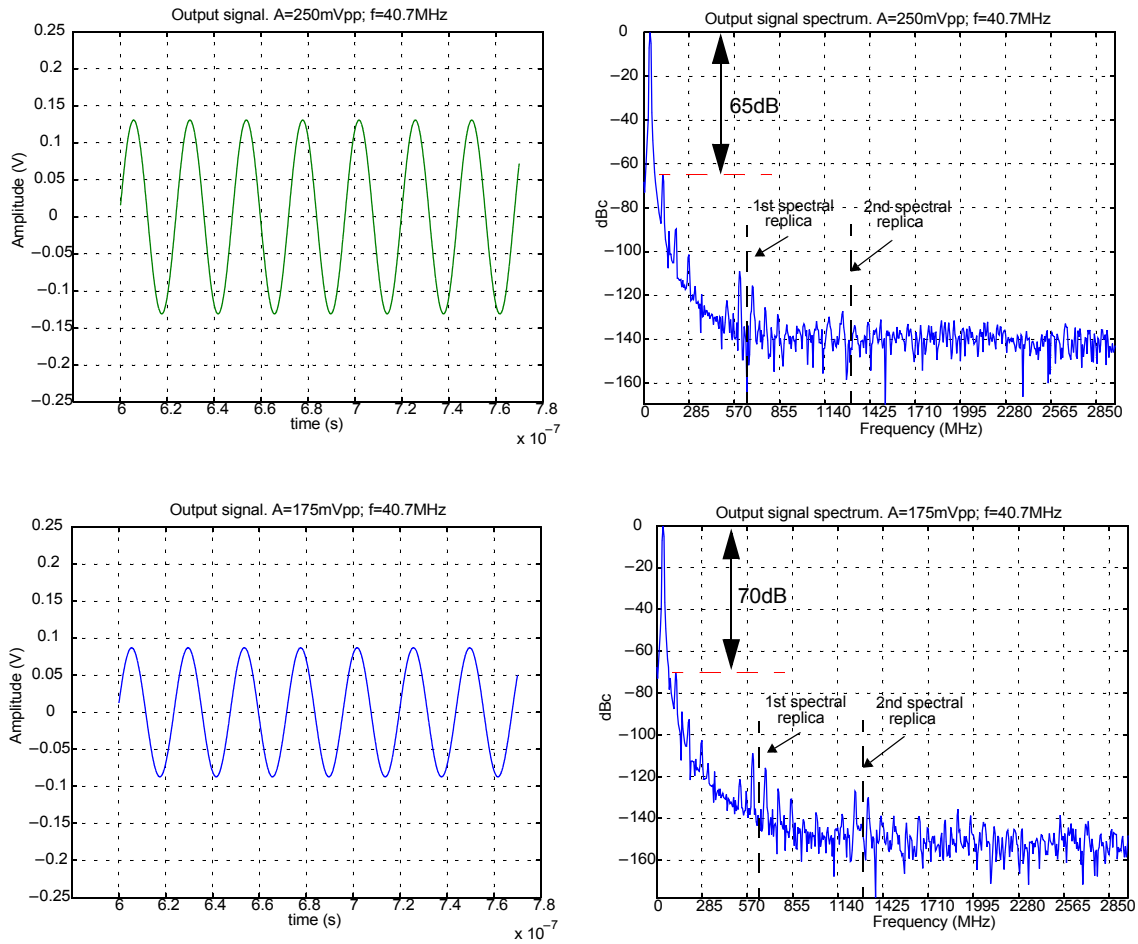
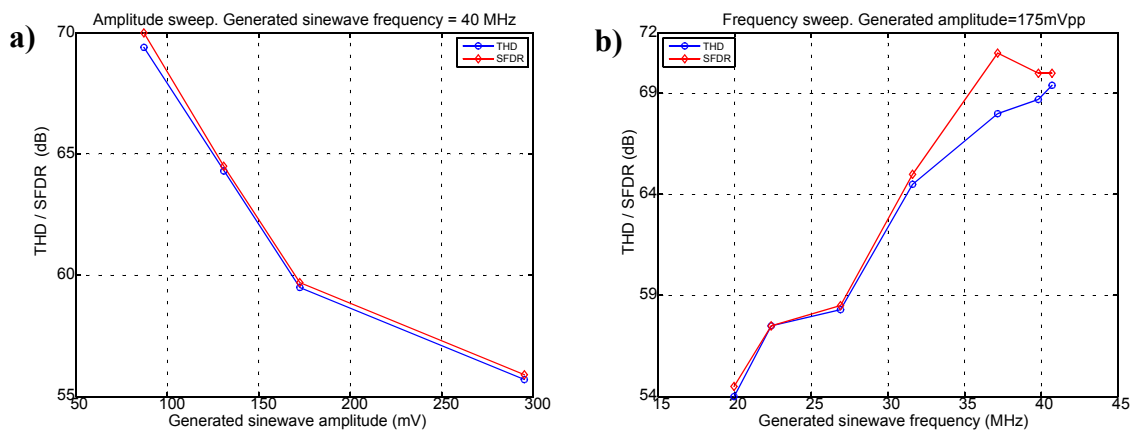


FIGURE 3.15. (cont.) Generator output signal: waveforms and spectra



**FIGURE 3.16. a) Generator output THD and SFDR as a function of the output amplitude. b) Generator output THD and SFDR as a function of the output frequency**



**TABLE 3.8. Obtained performance for the continuous-time generator**

Generated amplitude = 175mVpp			Generated frequency = 40.7MHz		
Frequency (MHz)	THD (dB)	SFDR (dB)	Amplitude (mVpp)	THD (dB)	SFDR (dB)
20	54	55	175	69	70
22.4	58	58	250	64	65
27	58	59	345	60	60
31.6	65	65	590	56	56
37.2	68	71			
39.8	69	70			
40.7	69	70			

As it is shown in Figure 3.16 and Table 3.8, the quality of the signal decreases with the amplitude due mainly to the limited linear range in the transconductors, and increases with the frequency because of the higher bias currents needed to increase the filter peak frequency. Obtained results meet the goal specifications defined in Table 3.1, and also agree very well with the expected performance. According to the high-level simulations, the main limiting factor is the linearity of the filter core.

### 3.3. SC prototype

This section details the design of a discrete-time sinewave generator based on the switched-capacitor technique using a  $0.35\mu\text{m}$ -3.3V CMOS technology. The objective, as it was the case with the OTA-C one, is to provide a prototype to validate the proposed technique and illustrate the design methodology. The general goal specifications for the SC generator, which are listed in Table 3.9, are typical performance parameters of SC filters in the mentioned technology.

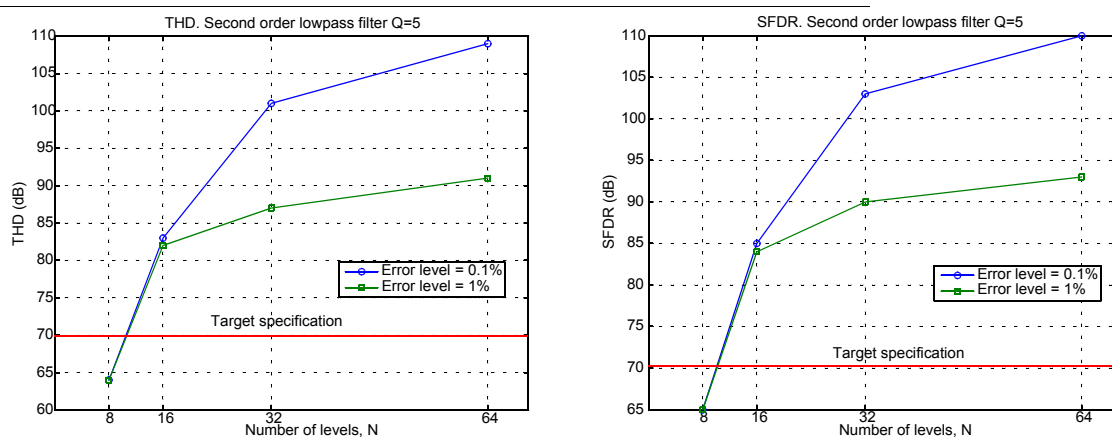
TABLE 3.9. Goal specifications

Parameter	Value
Frequency range	clock frequency up to 2MHz
Amplitude range	up to 1V peak-to-peak
Linearity	better than 70dB THD and SFDR in the desired frequency and amplitude range

#### 3.3.1. General considerations

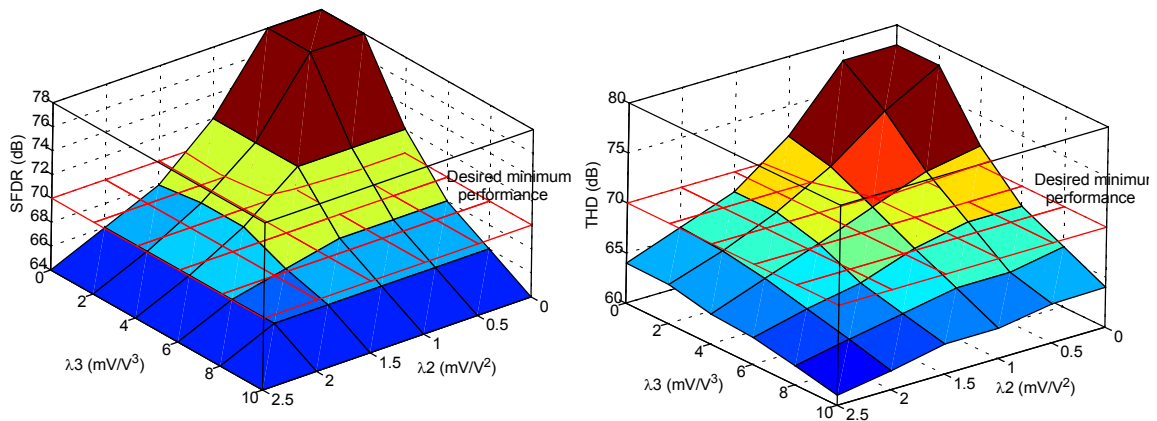
Again, the first design decision is to consider the trade-off between the characteristics of the function  $f(t)$  and the shape of the filtering stage, in the view of the desired specifications. Similarly to the OTA-C case, Figure 3.17 shows that the combination of a 16-step sinewave as function  $f(t)$  and a second-order lowpass filtering stage with a  $Q$  factor around  $Q=5$  represents a good trade-off solution which gives linearity figures above the goal specifications.

FIGURE 3.17. THD and SFDR estimation as a function of the number of step levels





**FIGURE 3.18. SFDR and THD estimations using a third-order model for a 1V<sub>pp</sub> signal. The plane at 70dB marks the desired minimum performance**



Concerning the linearity of the filtering stage, SC circuits usually provide better linearity performance than their OTA-C counterparts, due to the fact that their functionality is based on charge transfer between capacitors, and current CMOS technologies provide high quality capacitors and capacitor matching. Figure 3.18 shows an exploration of the design space in terms of the non-linear coefficients  $\lambda_2$  and  $\lambda_3$  previously defined. Assuming that coefficient  $\lambda_2$  can be made close to zero using a fully-differential architecture, the third-order coefficient  $\lambda_3$  has to be lower than  $5\text{mV/V}^3$  in the defined signal range in order to fulfill the desired linearity specifications in Table 3.9. In this case, the maximum error in the step levels that define  $f(t)$  has to be lower than 1% of its intended value to not to degrade the linearity figures. Unlike the OTA-C case, the higher linearity specifications impose a more restrictive value for the errors in the step levels. Fortunately, this error is related to the capacitor matching in the selected technology, and it is feasible in current CMOS technologies. Figure 3.19 shows the spectrum of the generator output obtained with the high level model under the discussed limit conditions of error level and linearity. The obtained result agrees with the goal specifications defined in Table 3.9.

Figure 3.20 shows a general block diagram of the proposed SC generator architecture. Like the OTA-C one, it consists of the selected second-order lowpass filter, whose input devices have been modified to generate the step-levels of a 16-step sinewave. The main difference with the OTA-C generator is that in the SC case there is no need of tuning circuitry. The central frequency of the filter core is set by design at an integer division of the master clock frequency, so it is then possible to achieve the tracking of the central frequency and the frequency of  $f(t)$  simply clocking the input elements with the appropriate division of the master clock.

FIGURE 3.19. Output spectrum obtained with the high level model for the limit case ( $N=16$ , error level=1%,  $\lambda_2=0$ ,  $\lambda_3=5\text{mV/V}^3$ , peak-to-peak output voltage=1V)

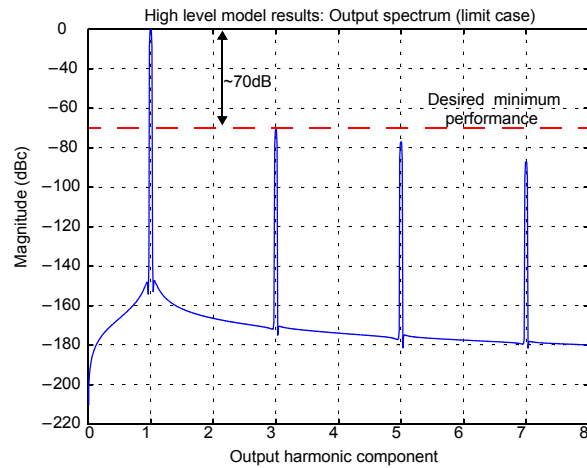


FIGURE 3.20. General block diagram of the proposed SC generation scheme

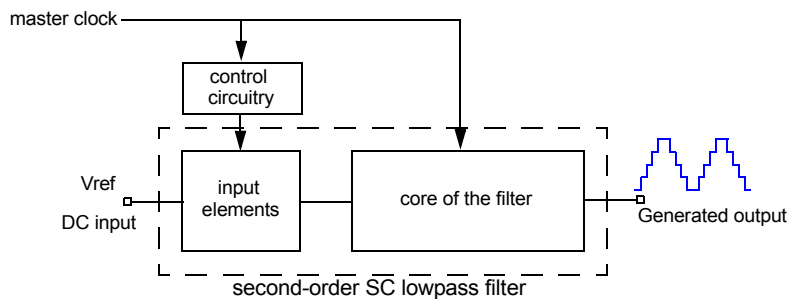
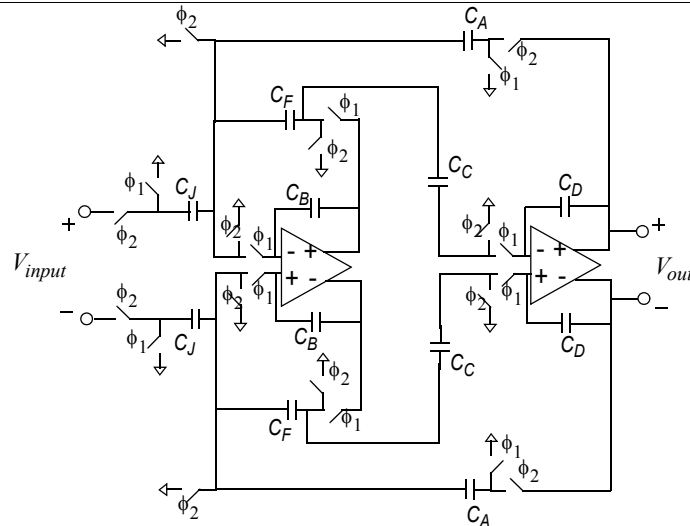


FIGURE 3.21. System level block diagram of the SC reference filter



### 3.3.2. System level

Let us discuss firstly the design of the reference filtering stage, and then we will discuss the modification of its input elements to build the desired sinewave generator.

#### A. Reference filter

The selected filter architecture is the well-known Fleischer-Laker biquad [55] in a fully-differential low-pass configuration, as shown in Figure 3.21. The filter operates with two non-overlapped clock phases  $\phi_1$  and  $\phi_2$ . The transfer function of the filter,  $T(z) = V_{out}(z)/V_{input}(z)$ , in the  $z$ -transform domain, valid in the  $\phi_1$  phase, is obtained by simple analysis,

$$T(z) = \frac{-C_D C_J z^{-1} + C_D C_J z^{-2}}{C_D (C_F + C_B) - (2C_D C_B - C_A C_C + C_D C_F) z^{-1} + C_D C_B z^{-2}} \quad (3.10)$$

To achieve a moderate peak gain while not limiting too much the input range of the filter, the peak gain of the filter is going to be set to 6dB. The pole quality factor is set to 5, to improve the selectivity of the filter near the passband edge. Finally, the central frequency will be set at one-sixteenth of the clock frequency. This choice for the central frequency will be useful to synchronize the variable input of the generator and the clock of the filter core. More details about this synchronization will be given in the following section. Table 3.10 lists the normalized capacitance

values for the capacitors in the reference filter to achieve the desired filter performance. The proposed design reduces the capacitance spread to 12.75.

**TABLE 3.10. Normalized capacitor values for the SC filter in Figure 3.21**

$C_A$	5.194	$C_D$	2.574
$C_B$	12.749	$C_F$	1.014
$C_C$	1	$C_J$	2

### B. SC sinewave generator

The system level block diagram of the discrete-time generator is shown in Figure 3.22a. The only modification with respect to the original reference filter is that the input capacitor  $C_J$  has been replaced by a switching scheme controlled by signal  $\phi_{in}$  and a programmable capacitor  $C_j(t)$ , that is composed by an array of four capacitors ( $C_{j1}$  to  $C_{j4}$ ) as depicted in Figure 3.22b, which are connected in parallel and to the signal path sequentially, according to the time scheme shown in Figure 3.22c (the generation of the programming signals is detailed in Appendix 1). Similarly to the OTA-C approach, this time-variant input scheme generates the required steps of a positive half sinewave, while the input switching scheme controlled by signal  $\phi_{in}$  in Figure 3.22c sets the weight (positive or negative) of the step. That is, the input capacitor can be described as,

$$C_j(t) = \{\phi_{in}(t) - \overline{\phi_{in}(t)}\} \left\{ \sum_{k=0}^4 c_k(t) C_{jk} \right\} \quad (3.11)$$

where,

$$C_{jk} = C_J \sin \frac{k\pi}{8} \quad k = 0, 1, \dots, 4 \quad (3.12)$$

Given that, by construction, the peak frequency of the filter core is one-sixteenth of the clock frequency, the output signal frequency and the peak frequency are coincident when the control signals in Figure 3.22c are synchronized to the same master clock used for the generation of filter core clock phases  $\phi_1$  and  $\phi_2$ . That is, in this case the frequency of the generated signal and the central frequency of the filter core are coincident by design.

FIGURE 3.22. a) Block diagram of the SC signal generator. b) Time-variant capacitor. c) Time scheme.

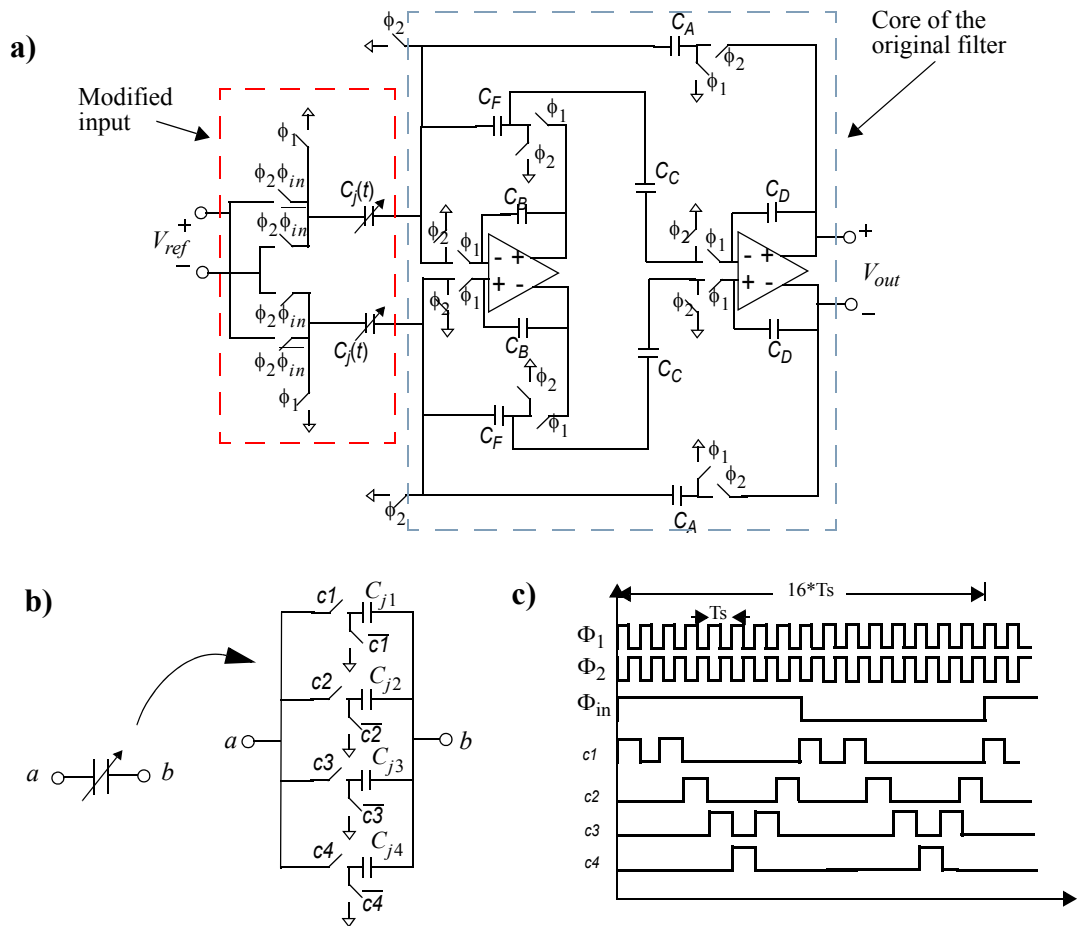
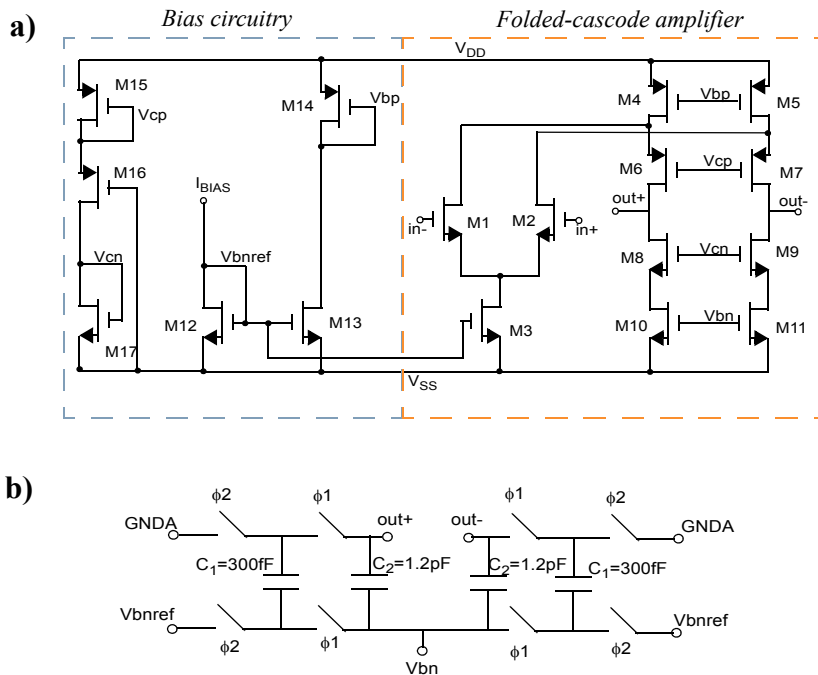


FIGURE 3.23. a) Fully-differential folded-cascode amplifier. b) Dynamic common mode feedback circuitry



### 3.3.3. Schematic level: design of the building blocks

#### *Amplifiers*

The selected amplifier architecture is a one-stage folded-cascode fully-differential amplifier. This kind of structure offers a good trade-off between gain and bandwidth. Moderate-to-high gain and bandwidth are possible, at the cost of a reduction of the output swing of the amplifier due to the cascode elements. Figure 3.23a shows the transistor level schematic of the amplifier together with its bias circuitry. The necessary common-mode feedback is provided by the dynamic circuit in Figure 3.23b [67]. This circuit senses the common mode output voltage and returns a signal through the bias line labelled  $V_{bn}$  to stabilize the common mode output voltage to analog ground. In addition, the 1.2pF capacitors connected to the output nodes ( $C_2$  in Figure 3.23b) provide the needed frequency compensation for the amplifier.

Table 3.11 lists the sizes of the transistors in Figure 3.23, while Table 3.12 shows the performance characteristics of the amplifier obtained by electrical simulation for biasing conditions  $V_{DD}=3.3\text{V}$ , and  $I_{BIAS}=60\mu\text{A}$ .

**TABLE 3.11. Transistor sizes for the amplifier in Figure 3.23**

	M1=M2	M3	M4=M5	M6=M7	M8=M9
<b>W (<math>\mu\text{m}</math>)</b>	100	96	180	180	96
<b>L (<math>\mu\text{m}</math>)</b>	1	1	2	1	1
	M10=M11	M12=M13	M14	M15=M16	M17
<b>W (<math>\mu\text{m}</math>)</b>	48	16	30	5	2.6
<b>L (<math>\mu\text{m}</math>)</b>	1	1	2	4	4

**TABLE 3.12. Amplifier performance parameters ( $V_{DD}=3.3\text{V}$ ,  $I_{BIAS}=60\mu\text{A}$ )**

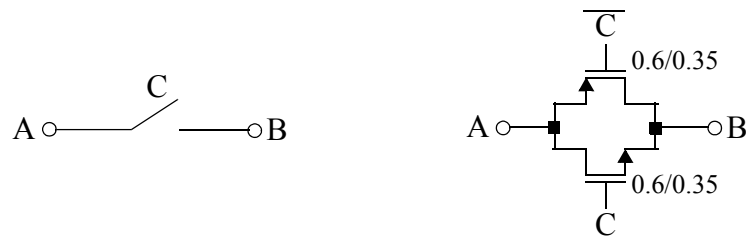
<b>DC gain</b>	80dB
<b>Gain-bandwidth product</b>	180MHz
<b>Phase margin</b>	55°
<b>Settling time (1%)</b>	4.0ns
<b>Slew-rate</b>	170V/ $\mu\text{s}$

#### *Switches and capacitors*

Typical minimum size CMOS switches have been adopted to reduce clock feedthrough effects. Figure 3.24 shows the transistor level schematic of the designed switches.

Concerning the capacitors, they are designed following general design guidelines to improve matching. Thus, the capacitance values in Table 3.10, together with the capacitors composing the common-mode feedback circuitry of the amplifiers, are built from combinations of unit polysilicon capacitors  $C_u$  in parallel. This unit element has been set to a  $19\mu\text{m} \times 19\mu\text{m}$  double-poly capacitor, which corresponds to a capacitance of about 300fF. Table 3.13 lists the number of unit capacitors used for each of the capacitors composing the system. Note that since the relations in Table 3.10 are not integer, capacitors slightly bigger or smaller than  $C_u$  have been added when needed to achieve the desired capacitor ratios.

FIGURE 3.24. Minimum size CMOS switch

TABLE 3.13. Building the capacitors with unit elements ( $C_u$  is a  $19\mu\text{m} \times 19\mu\text{m}$  capacitor)

	Capacitor	Composition	Capacitor	Composition
Filter capacitors	$C_A$	$4C_u + \text{a } 19\mu\text{m} \times 22.7\mu\text{m}$ capacitor	$C_D$	$2C_u + \text{a } 19\mu\text{m} \times 10.8\mu\text{m}$ capacitor
	$C_B$	$12C_u + \text{a } 19\mu\text{m} \times 14.2\mu\text{m}$ capacitor	$C_F$	$\text{a } 19\mu\text{m} \times 19.25\mu\text{m}$ capacitor
	$C_C$	$1C_u$	$C_J$	$2C_u$
CMFB capacitors	$C_1$	$1C_u$		
	$C_2$	$4C_u$		

*Input programmable input capacitor*

Capacitors  $C_{j1}$  to  $C_{j4}$  have been sized to get the desired capacitance values defined by (3.12). Table 3.14 registers the sizes of these elemental capacitors. To improve matching the capacitance values have been obtained by parallel combinations of the already defined unit polysilicon capacitor  $C_u$  ( $19\mu\text{m} \times 19\mu\text{m}$ ) when possible.



**TABLE 3.14. Realization of the input capacitors with unit elements**

Capacitor	Composition
$C_{j1}$	a $19\mu\text{m} \times 14.5\mu\text{m}$ capacitor
$C_{j2}$	$1C_u$ + a $19\mu\text{m} \times 7.7\mu\text{m}$ capacitor
$C_{j3}$	$1C_u$ + a $19\mu\text{m} \times 16\mu\text{m}$ capacitor
$C_{j4}$	$2C_u$

Monte Carlo models in the selected technology predict possible deviations in the desired capacitance values  $C_{j1}$  to  $C_{j4}$  below 0.2% for the capacitor sizes listed in Table 3.14. According to our previous design considerations, this assures that the performance of the generator will not be limited by the accuracy of the capacitance step values.

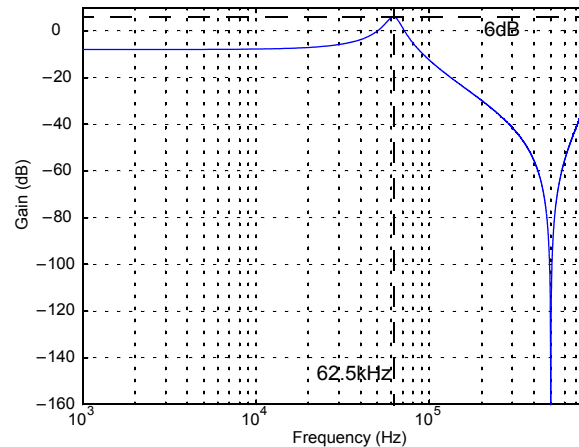
*Complete filter: electrical simulation results at schematic level*

Once the design of the building blocks is completed, an electrical simulation of the whole filter is performed to check the fulfillment of the target specifications. For the simulations the clock frequency has been set to 1MHz. The results of the simulations are registered in Table 3.15, and the magnitude response of the filter is shown in Figure 3.25.

**TABLE 3.15. Performance parameters of the reference filter**  
( $V_{DD}=3.3\text{V}$ ,  $I_{BIAS}=60\mu\text{A}$ , master clock frequency=1MHz)

<b>DC-gain</b>	-8dB
<b>Peak frequency @ <math>f_{clk}=1\text{MHz}</math></b>	62.5kHz
<b>Peak gain</b>	6dB
<b>THD @ peak frequency; 1Vpp</b>	84dB
<b>SFDR @ peak frequency; 1Vpp</b>	86dB

FIGURE 3.25. Magnitude response of the reference filter



The obtained linearity performance corresponds, in the previously discussed polynomial model, to a  $\lambda_3$  coefficient about  $\lambda_3=0.3\text{mV/V}^3$  in the selected signal range, which, together with the 0.2% maximum variation of the input step levels for the programmable input capacitor, is in agreement with the goal linearity specifications for the desired generator.

### 3.3.4. Layout level and post-layout simulations

The SC generator prototype has been laid out following the recommended guidelines for switched-capacitor circuits. Analog amplifiers are separated from the switches and digital circuitry by the capacitor array. Figure 3.26 shows a diagram of the design floor-planning together with the layout of the system. It occupies an area of  $280\mu\text{m} \times 550\mu\text{m}$ .

FIGURE 3.26. Floor-planning and layout of the discrete-time SC sinewave generator



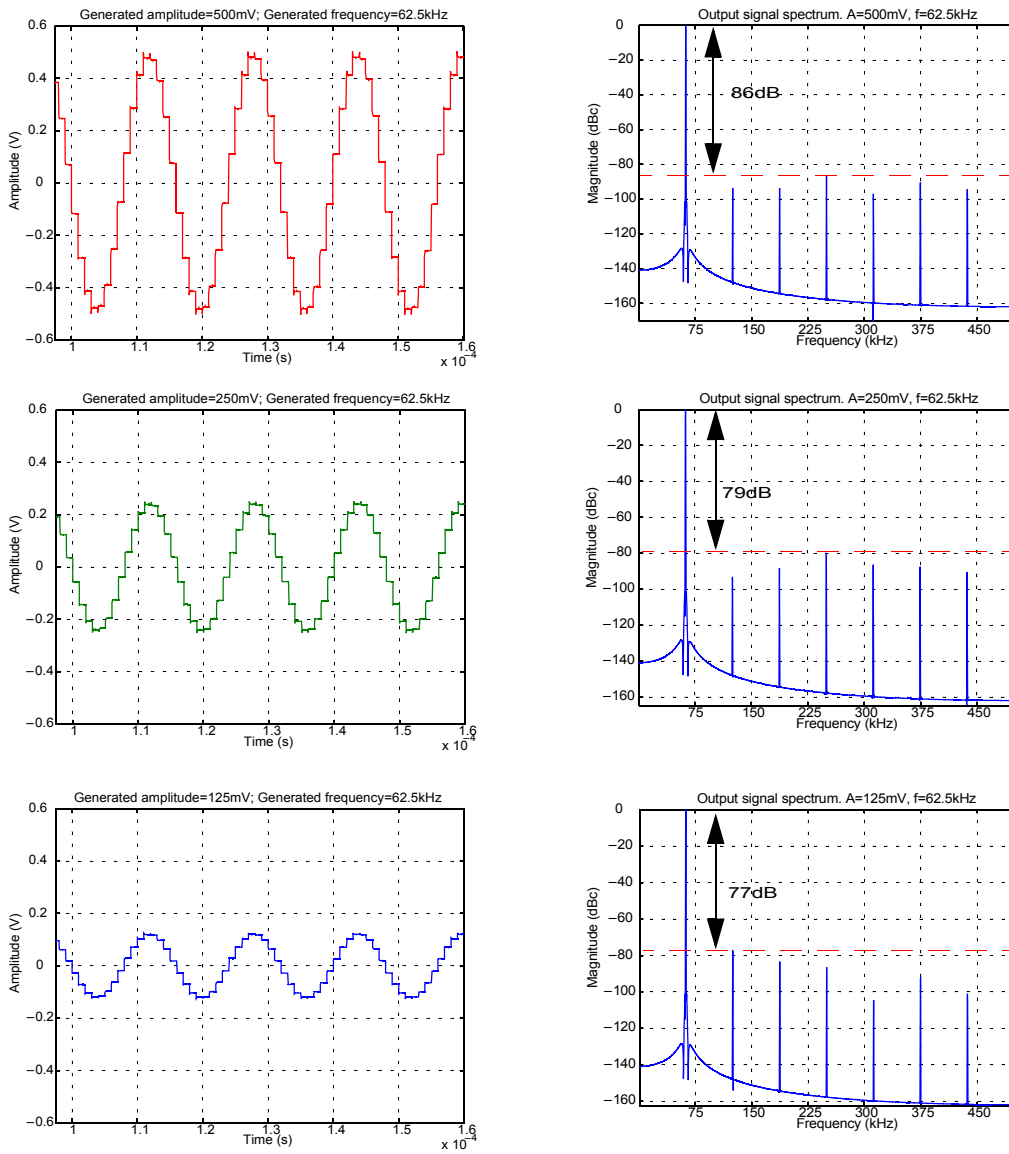
Post-layout simulations of the generator extracted view were performed. Firstly, as in the continuous-time case, the performance of the filter core is checked. For this purpose, control signals  $c_1$ ,  $c_2$ , and  $c_3$  are set to a logic '0', while signals  $c_4$  and  $\phi_{in}$  are set to a logic '1'. In this configuration, the system is equivalent to the discrete-time SC reference filter previously described. Table 3.16 shows the obtained performance parameters. As it can be seen by the results, the performance of the filter core agrees very well with the expected performance of the reference filter.

**TABLE 3.16. Performance parameters of the system when configured as the reference filter ( $V_{DD}=3.3V$ ,  $I_{BIAS}=60\mu A$ , master clock frequency=1MHz)**

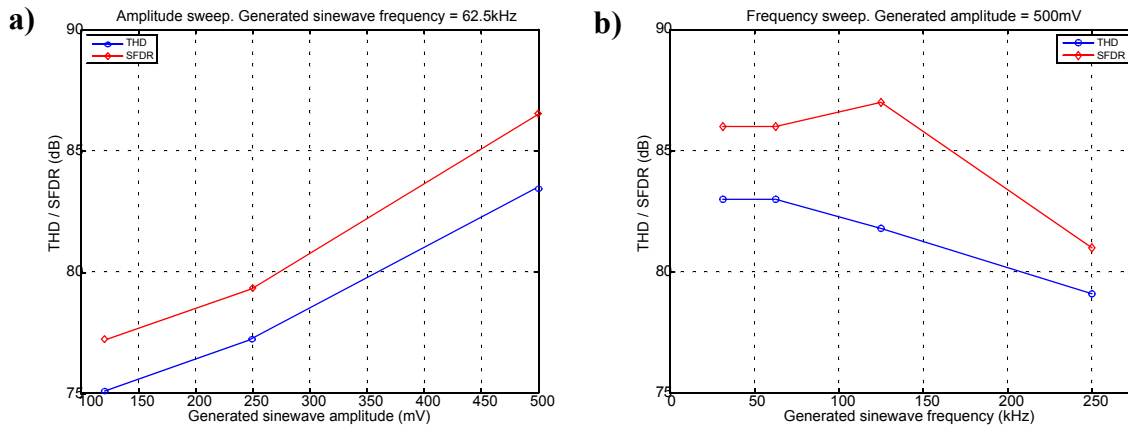
<b>DC-gain</b>	-8dB
<b>Peak frequency @ fclk=1MHz</b>	62.5kHz
<b>Peak gain</b>	6dB
<b>THD @ peak frequency; 1Vpp</b>	83dB
<b>SFDR @ peak frequency; 1Vpp</b>	86dB

Once the performance of the filter has been verified, the sinewave generator is simulated. Figure 3.27 shows three output waveforms and their spectra, obtained by electrical simulation of the generator extracted view. In this simulations the clock frequency has been set to 1MHz, which gives an output signal at 62.5kHz, while its peak-to-peak amplitude has been swept from 1V to 250mV. In terms of spectral purity, the achieved THD in this amplitude range keeps approximately between 83dB and 75dB, while the SFDR is between 86dB and 77dB. The even harmonics are due to parasitic contributions that unbalance the fully-differential architecture. Figure 3.28 and Table 3.17 show the performance parameters obtained in another set of simulations when sweeping both the amplitude and the frequency of the generated signal.

FIGURE 3.27. Generator output signals



**FIGURE 3.28. a) SC-generator output THD and SFDR as a function of the output amplitude. b) SC-generator output THD and SFDR as a function of the output frequency**



**TABLE 3.17. Obtained performance for the discrete-time generator**

Generated amplitude = 500mV			Generated frequency = 62.5kHz		
Frequency (kHz)	THD (dB)	SFDR (dB)	Amplitude (mV)	THD (dB)	SFDR (dB)
15.6	82	86	125	75	77
31.25	83	86	250	77	79
62.5	83	86	500	83	86
125	82	87			
250	79	81			

The obtained results meet the goal design specifications defined in Table 3.9, and also agree very well with the expected performance.

### 3.4. Prototype characterization

The developed OTA-C and SC generators were fabricated in the selected  $0.35\mu\text{m}$  CMOS technology. Figure 3.29 shows microphotographs of the integrated sinewave generators. As addressed before, the OTA-C generator occupies an area of  $395\mu\text{m} \times 230\mu\text{m}$ , while the SC one occupies  $280\mu\text{m} \times 550\mu\text{m}$ , excluding pads in both cases.

This section summarizes the most significant experimental results obtained from these integrated prototypes to illustrate the feasibility and performance of the approach.

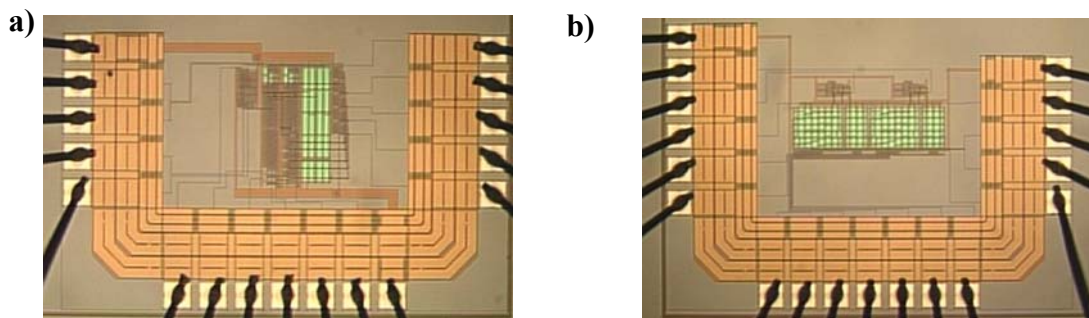
#### 3.4.1. OTA-C Prototype

##### *A. Test set-up for the OTA-C generator*

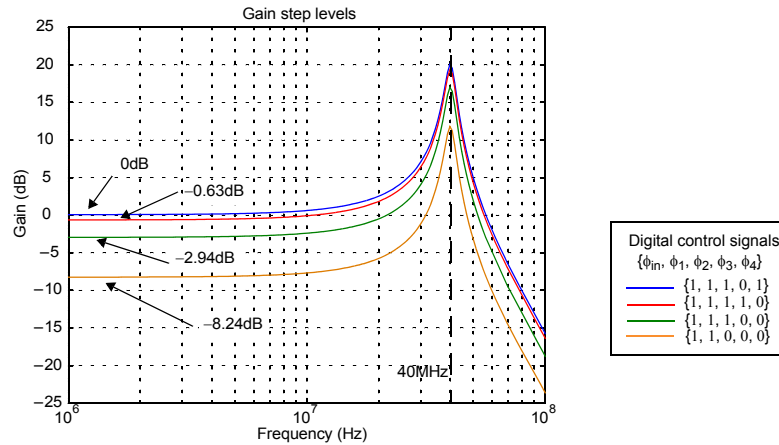
We opted to perform indirect measurements to validate the functionality of the prototype because the test equipment to generate the needed control signals at the required frequency (i. e. 640MHz clock frequency for a 40MHz output signal) was not available in our laboratory facilities.

The prototype was characterized as a filter using a network analyzer in the four gain configurations that define the step levels of the stepwise sinewave, and THD and SFDR measurements were performed with the system configured as the reference filter. These data allows to give an estimation of the performance that can be achieved by the OTA-C generator.

FIGURE 3.29. Microphotographs: a) Integrated OTA-C prototype; b) Integrated SC prototype



**FIGURE 3.30. Gain steps for the different control signal configurations**  
**( $I_B=200\mu\text{A}$ ,  $V_{DD}=3.3\text{V}$ )**



### B. Experimental results

Firstly, the four different gain step levels of the system were measured. For that, the set of digital control signals  $\{\phi_{in}, \phi_1, \phi_2, \phi_3, \phi_4\}$  was fixed to the corresponding gain step level, and the magnitude response of the filter was extracted for each configuration. Figure 3.30 shows the obtained Bode magnitude responses, together with the corresponding DC-gain of each step. The biasing conditions were set to  $I_B = 200\mu\text{A}$  and  $V_{DD} = 3.3\text{V}$ , which gives a peak-gain frequency of 40MHz.

Secondly, the system was configured as the reference filter and its linearity in terms of THD and SFDR was characterized when excited by a 250mV peak-to-peak sinusoidal stimulus at the peak-gain frequency. Table 3.18 shows the obtained results.

**TABLE 3.18. Performance parameters of the OTA-C generator when configured as the reference filter (Output amplitude = 250mVpp)**

Bias conditions	$V_{DD}=3.3\text{V}; I_B=200\mu\text{A}$	$V_{DD}=3.3\text{V}; I_B=45\mu\text{A}$
DC-gain	0dB	0dB
Peak frequency	40MHz	20MHz
Peak gain	19dB	19dB
THD @ peak frequency	62dB	50dB
SFDR @ peak frequency	64dB	52dB

The obtained results summarized in Figure 3.30 and Table 3.18 allow to make an estimation of the performance of the OTA-C generator prototype. For this purpose, the extracted gain levels, Bode gain diagrams and linearity figures were used to model the system according to the high-level model proposed in the previous section. Table 3.19 shows the performance parameters of the OTA-C generator estimated by the developed model.

**TABLE 3.19. Estimation of the OTA-C generator performance**

<b>Generated Frequency</b>	40MHz	20MHz
<b>Generated amplitude</b>	250mVpp	250mVpp
<b>THD</b>	62dB	50dB
<b>SFDR</b>	64dB	52dB

The estimated performance shows that the main limitation in terms of linearity is given by the linearity of the reference filter. This is in agreement with the results obtained in the simulations of the extracted view given in the previous section.

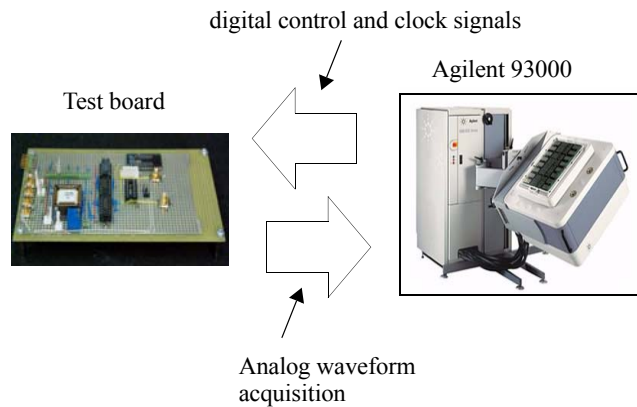
### 3.4.2. SC Prototype

#### *A. Test set-up for the SC generator*

The general test set-up is depicted in Figure 3.31. It makes use of the mixed-signal test system Agilent 93000. This test system generates the digital control signals and clock, provides the supply and analog reference voltages, and acquires and processes the output of the generator under test. Although the selected test system has many advantages in terms of flexibility, reprogrammability, and automation, it has an important limitation for our intended measurements. The digitizer board mounted on the Agilent test system, that acquires the analog output signal of the generator, features a 12bit resolution A/D converter, with 75dB THD (typical value in specific loading conditions) at 1MHz [68]. These figures are below the performance obtained by simulations of the generator. It is then expected that our test set-up will limit our measurements. At the moment of writing this document, the lack of alternative test equipment in the desired range of frequency and resolution forced us to accept this limitation.



FIGURE 3.31. General test set-up



B. Experimental results

A set of experiments has been developed to test the functionality of the sinewave generator, and prove the feasibility of the approach.

Figure 3.32 shows four output waveforms from the sinewave generator and their corresponding spectra. The frequency of these signals is fixed to 62.5kHz (1MHz clock frequency). Their amplitudes are 300mV, 400mV, 500mV, and 600mV, corresponding to the reference voltages 150mV, 200mV, 250mV, and 300mV, respectively. The spectra were evaluated taking one sample per clock cycle.

Figure 3.33 details THD and SFDR measurements as a function of the output amplitude for a given signal frequency (Figure 3.33a), and as a function of the output frequency for a given signal amplitude (Figure 3.33b). As it can be deduced from Figure 3.33 the quality of the signal is approximately constant over the whole operational range of the generator. Table 3.20 details the obtained performance parameters when sweeping both the generated frequency and amplitude.

FIGURE 3.32. Generator output signals

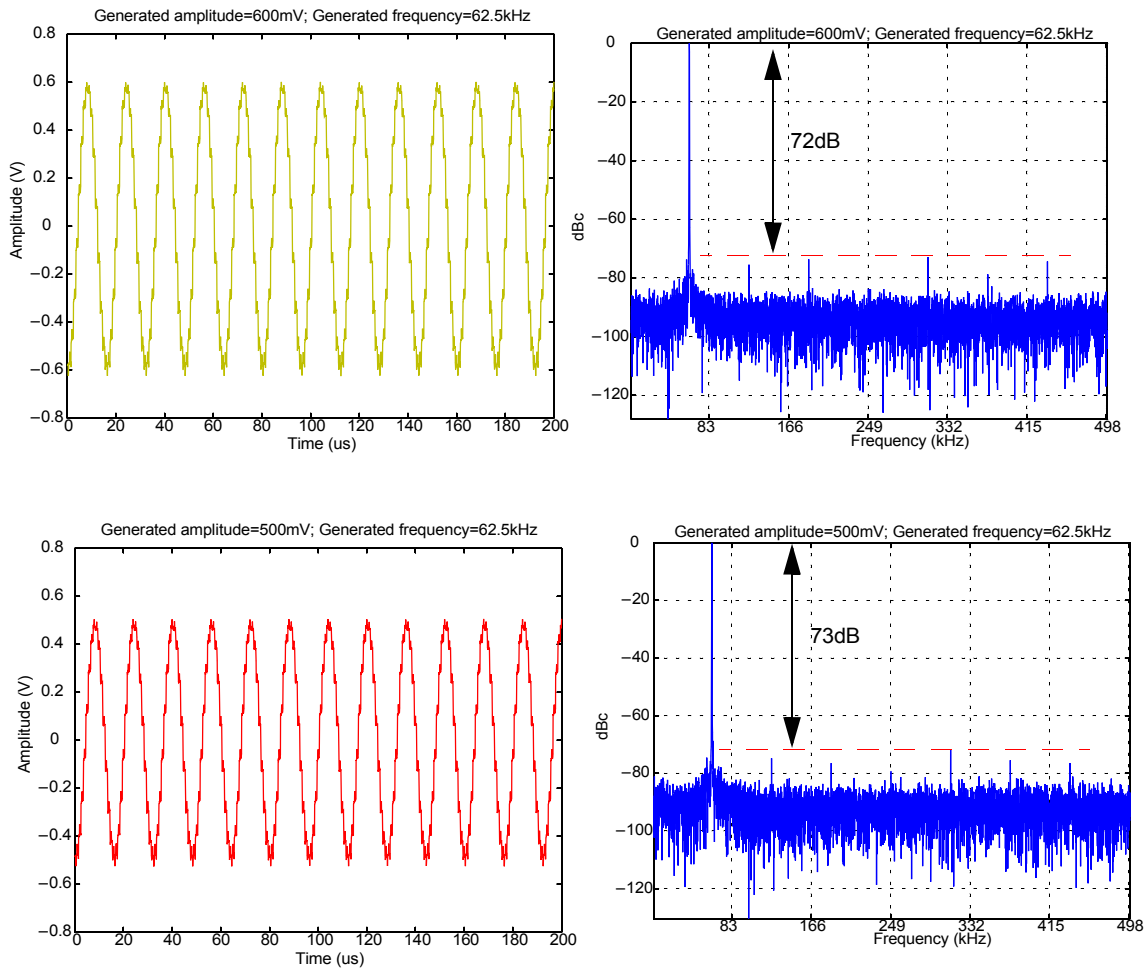
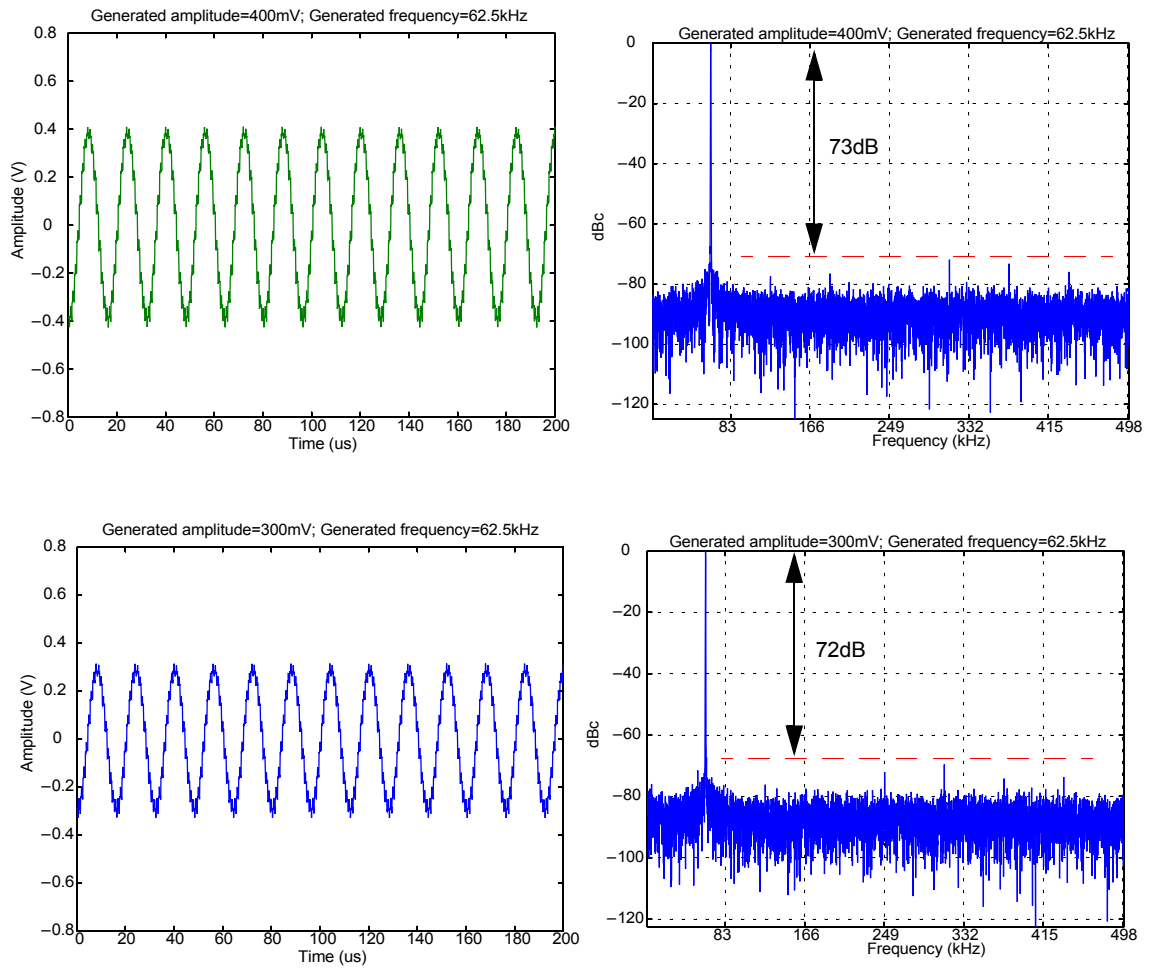
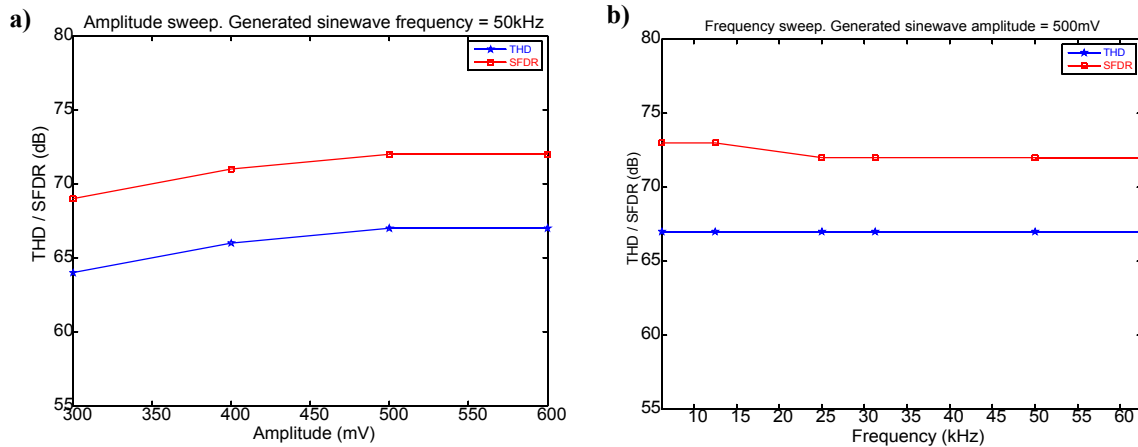


FIGURE 3.32. (cont.) Generator output signals



**FIGURE 3.33. a) Generator output THD and SFDR as a function of the output amplitude.  
b) Generator output THD and SFDR as a function of the output frequency**



**TABLE 3.20. Obtained performance for the discrete-time generator**

Generated amplitude = 300mV			Generated amplitude = 400mV		
Frequency (kHz)	THD (dB)	SFDR (dB)	Frequency (kHz)	THD (dB)	SFDR (dB)
6.25	67	72	6.25	67	73
12.5	67	72	12.5	67	71
25	68	71	25	67	72
31.25	67	70	31.25	68	73
50	64	69	50	66	71
62.5	65	69	62.5	67	72

Generated amplitude = 500mV			Generated amplitude = 600mV		
Frequency (kHz)	THD (dB)	SFDR (dB)	Frequency (kHz)	THD (dB)	SFDR (dB)
6.25	67	73	6.25	67	72
12.5	67	73	12.5	68	73
25	67	72	25	67	73
31.25	67	72	31.25	69	75
50	67	72	50	67	73
62.5	67	72	62.5	67	72

The obtained results show the functionality and feasibility of the proposed approach. Concerning the performance of the approach, the obtained performance parameters are a reflection of the limitations imposed by our test set-up. The employed digitizer board features a 12-bit A/D converter with performance figures close to the obtained results. This limitations is obvious in the fairly constant figures that have been measured all over the frequency and amplitude ranges, and agrees very well with the performance of the digitizer board stated by its manufacturer.

### 3.5. Summary

Two practical implementations of the proposed sinewave generation scheme have been presented and discussed. Both implementations are mainly reduced to a second-order lowpass filter with a relatively small  $Q$  factor, whose input elements have been slightly modified. Namely, a continuous-time sinewave generator based on the OTA-C technique and a discrete-time one based on a SC filter have been developed and integrated in a standard  $0.35\mu\text{m}$  CMOS technology.

Practical measurements in the lab show the feasibility of the approach. Table 3.21 and Table 3.22 show a comparison with other reported solutions for analog signal generation in the continuous-time and discrete-time domains respectively.

**TABLE 3.21. Comparison with other continuous-time generation schemes**

	Continuous-time oscillator [69]	Analog $\Sigma\Delta$ oscillator [48]	RAM-based generator [45]	Proposed approach: OTA-C generator*
<b>Technology</b>	$0.8\mu\text{m}$ CMOS	FPGA	$0.8\mu\text{m}$ BiCMOS	$0.35\mu\text{m}$ CMOS
<b>Area</b>	$0.63\text{ mm}^2$	-----	$0.63\text{ mm}^2 +$ 4th-order filter	$0.1\text{ mm}^2$
<b>THD</b>	44dB@25MHz	84dB@5kHz	not reported	62dB@40MHz
<b>SFDR</b>	49dB@25MHz	86dB@5kHz	65dB@1MHz	64dB@40MHz

\*. Performance parameters obtained by indirect measurements

**TABLE 3.22. Comparison with other discrete-time generation schemes**

	SC oscillator [70]	Step-wise generator [52]	Proposed approach: SC generator*
<b>Technology</b>	$0.35\mu\text{m}$	$0.5\mu\text{m}$ CMOS	$0.35\mu\text{m}$ CMOS
<b>Area</b>	$0.13\text{ mm}^2$	$0.09\text{ mm}^2$	$0.15\text{ mm}^2$
<b>THD</b>	58dB@1MHz	49dB@1kHz	67dB@62.5kHz
<b>SFDR</b>	60dB@150kHz	38dB@10kHz	72dB@62.5kHz

\*. Performance limited by the experimental set-up

Rather than a direct comparison between very different techniques, Table 3.21 and Table 3.22 are aimed to put the obtained results into perspective. Concerning the continuous-time generation domain, the analog  $\Sigma\Delta$  oscillator in [48] gives the best performance figures, but at the cost of a higher circuit complexity (a 6th order Butterworth lowpass filter is used to cancel the quantization noise). The continuous-time analog oscillator presented in [69] is a voltage controlled oscillator based on OTA-C analog filtering techniques. The RAM based generator in [45] makes use of  $\Sigma\Delta$  encoding schemes to generate analog test signals. It offers comparatively high linearity figures and it is mostly digital, but needs also a selective analog filter (a 4th order lowpass filter) to remove the shaped noise. Finally, our proposed continuous-time OTA-C generator offers a good trade-off between performance and circuit complexity. While the required circuitry is mainly reduced to a 2nd order lowpass filtering, it offers comparatively high linearity figures. In the discrete-time case, although the demonstrated performance is limited by the experimental conditions, the obtained performance figures compare very well with the analog SC oscillator reported in [70], and represent a significative improvement with respect to the step-wise generator reported in [52], at the cost of a slightly higher silicon area.

The low area overhead and low design effort of the developed generation strategy make it very suitable for analog/mixed-signal BIST applications demanding a high quality sinewave as test stimulus.





## On-Chip Characterization of Analog Periodic Signals

*This chapter presents a scheme for the evaluation of analog periodic signals based on an approximation of the Fourier series expansion. Its proposed implementation is based on a double modulation, square-wave and sigma-delta, together with a very simple digital processing algorithm. The developed technique extracts, in the digital domain, the main characteristics parameters of an analog periodic signal, such as its DC level, and the amplitude and phase of its harmonic components. The simplicity and robustness of the approach make it very suitable for BIST applications.*

## 4.1. Introduction

The characterization of analog periodic signals is a major key point in mixed-signal test. These test schemes are traditionally based on the application of a stimulus to the DUT, and the posterior characterization of the test response.

In this chapter we are going to focus on the on-chip characterization of periodic analog signals, with a special interest in BIST applications. Most of the analog and mixed-signal subsystems can be functionally tested and characterized by applying a periodic stimulus and processing the output response. This way, frequency related specifications, linearity parameters, etc, are usually extracted. Furthermore, the characterization of analog periodic signals is also a key point in the so-called Oscillation-Based Test (OBT) [71]. This test scheme consists of converting the DUT into an oscillator by reconfiguration during the test phase in such a way that the oscillation parameters (amplitude, frequency, DC-level, etc.) are directly related to the circuit behavior and performance during normal operation. A malfunction of the DUT can be detected through the characterization of the oscillating output signal [72]-[75]. The development of an on-chip approach for the characterization of periodic analog signals represents a crucial advance for integrating these known test solutions into a full BIST scheme.

This chapter is organized as follows. Firstly, Section 4.2 makes a brief review of different techniques that have been proposed in the literature for the characterization of analog periodic signals. Section 4.3 presents our proposal for the on-chip characterization of this kind of signals, and details its possible implementations. After that, Section 4.5 discusses some practical aspects about the feasibility of the proposed implementation. Finally, Section 4.6 highlights the key points of this chapter.

## 4.2. Review of previous techniques

A periodic signal is fully characterized by the set of its spectral components, that is, its DC level and the magnitude and phase of its harmonic components. The Fourier Transform is the standard tool for this purpose, and the Fast Fourier Transform (FFT) has become the standard algorithm used for its evaluation. It gives very accurate results and allows the decomposition of finite length signals into a set of harmonic frequency components. This algorithm, performed after a digital conversion of the signal, is the standard signal analysis method in most commercial ATEs (see Figure 4.1).

Besides test equipment based on the FFT algorithm, usual commercial equipment for the spectral characterization of analog signals also includes analog spectrum analyzers. These systems achieve the decomposition of the test signal into its harmonic components based on analog processing.

FIGURE 4.1. Standard FFT-based scheme for spectral measurements

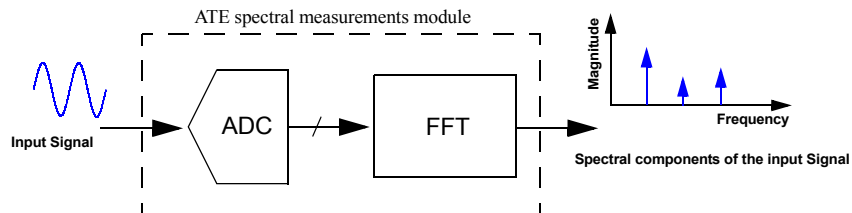
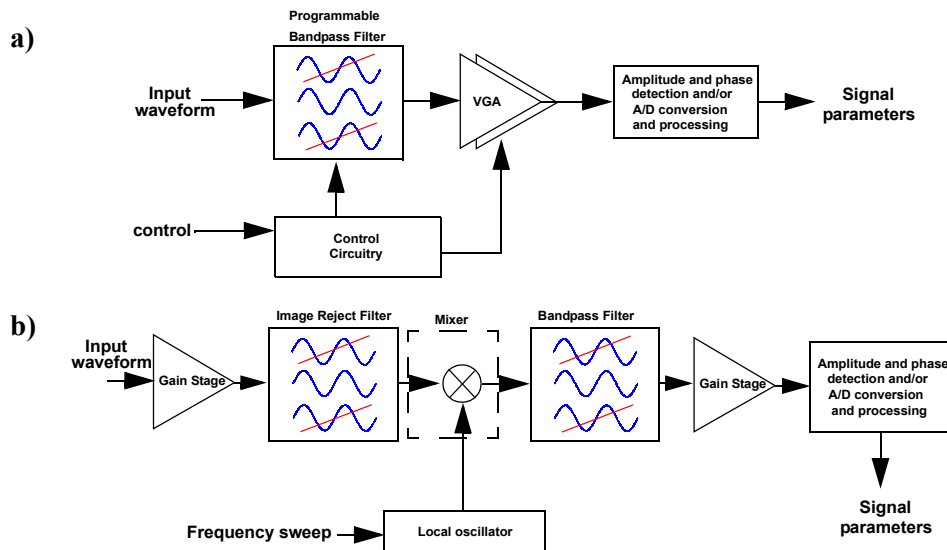


FIGURE 4.2. General scheme of an analog spectrum analyzer: a) based on filtering; b) based on modulation



Attending to the evaluation strategy, there are two basic kinds of analog spectrum analyzers: filter-based and modulation-based. A typical filter-based spectrum analyzer is shown in Figure 4.2a. It relies on an adjustable bandpass filter (or on a bank of filters) to extract information about the frequency content of the input signal. On the other hand, modulation-based ones make use of analog multipliers in a heterodyne configuration, as it is shown in Figure 4.2b, where the local oscillator sweeps the frequency range of interest.

The adaptation of these characterization methods to an efficient on-chip application represents a capital issue for the integration of analog and mixed-signal BIST schemes. Many interesting works have paid attention to this topic, and many different strategies have been presented [52],[70],[76]-[87].

Some approaches for the on-chip characterization of analog signals adapt the functionality of commercial spectrum analyzers and ATEs. For instance, the works in [52] and [70] present two on-chip filter-based spectrum analyzers suitable for BIST applications, while the work in [76] deals with the adaptation of a modulation-based spectrum analyzer for its on-chip implementation. In these approaches the signal processing is done mostly in the analog domain. This means that the processing circuitry is in general sensitive to process variations, environmental noise, loading effects, etc, which may degrade the performance of the system. In addition, the design of the analog blocks for signal processing is not always straightforward, demanding also a high design effort if the test core has to be migrated to different technologies.

Because of the shortcomings of purely analog approaches, many works on this particular topic prefer to move the processing of the signal to the digital domain and minimize the analog area, that is usually reduced to an A/D conversion [77]-[87]. There are two key points to be considered in the development of these digital approaches: the digital signal processing algorithm itself, and the unavoidable A/D interface.

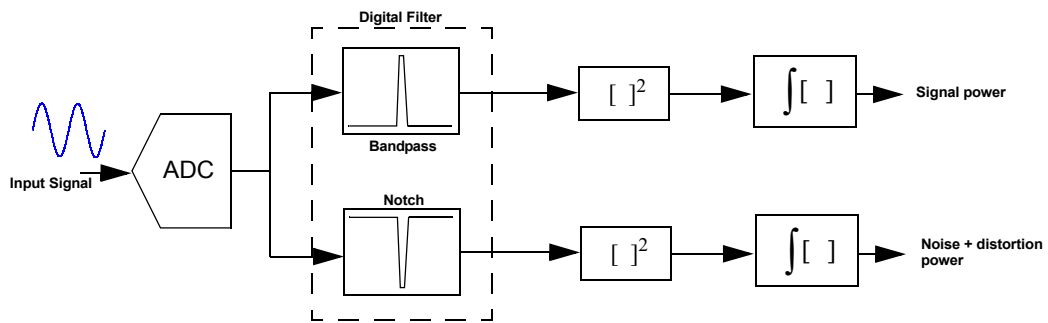
The adaptation of the FFT algorithm after an A/D conversion of the signal is a common approach. However, the direct on-chip implementation of the FFT, if  $N$  samples are considered, would demand  $N$  memory elements to store the samples, and would also require on the order of  $M\log(N)$  arithmetical operations. Since the accuracy of the measurements depends on the number of samples to be evaluated, an on-chip implementation is normally not practical due to an excessive overhead. It can be considered only if the needed resources are already available on-chip and can be reused during test mode. The work in [79] focus on this overhead issue and presents an FFT approximation technique, suitable for analog BIST applications, at the cost of a lower accuracy.

In the case there is only one frequency of interest, a sinewave fitting algorithm may be a good alternative to the FFT [80]. In terms of computational effort, this method is less expensive and more suitable for on-chip implementation. However, it requires memory elements to store sine functions what means large area requirements for a good accuracy.

Optimized algorithms as an alternative to the FFT algorithm have been also explored. For instance, the work in [81] makes use of the Goertzel algorithm. This algorithm, mostly used in telecommunication systems for the detection of dual-tone multi-frequency signals, is particularly suitable for applications demanding the evaluation of few spectral lines.

The use of digital filters is proposed in [82]. Figure 4.3 shows a block diagram of the approach. A digital filter provides two outputs, a bandpass function and its complementary notch function. For a given frequency, the power of the signal and the noise can be obtained by squaring and adding the bandpass and the notch outputs, respectively. The accuracy obtained with this approach depends on the selectivity of the filters and the number of samples. However it must be taken into account that the time required to obtain the measurement is larger while larger is the selectivity of the filter.

FIGURE 4.3. A simple parameter extractor based on digital filters



Usually, the main limitation of these digital algorithms is the analog to digital conversion that has to be introduced in the test core. An extra A/D converter has to be included if it is not possible to reuse an existing one. This converter effectively limits the performance of the test core, its design may be challenging if a high accuracy is needed, and it demands also self-test and/or calibration capabilities to prevent a possible malfunction. Many interesting works try to simplify this analog to digital conversion to develop efficient A/D converters for test applications.

The work in [83] deals with an on-chip test core featuring a periodic wave digitizer that can capture periodic analog signals at an effective sample rate of 4GHz through subsampling. However, the subsampling is based on the use of complex DLL blocks, what may compromise the feasibility of the system. Furthermore, the presented A/D interface requires the usual external digital processing (DFT, FFT, etc.) to extract the targeted signal parameter.

The strategy described in [84] presents a simplified A/D interface. It is based on the statistical properties of the signal under evaluation, in such a way that only a noise generator, a statistical sampler, and some digital processing are required to estimate the spectrum of the input signal. Nevertheless, it needs very large oversampling ratios that may compromise its application.

The use of  $\Sigma\Delta$ -modulators as analog response extractors has been proved to be useful [85]-[87]. The main advantages of these  $\Sigma\Delta$ -based approaches are the simplicity and the robustness of the required circuitry, which make them very suitable for on-chip implementation, and hence, for BIST applications.

The work in [87] presents a simple  $\Sigma\Delta$ -based approach for the extraction, in the digital domain, of the frequency, amplitude, and DC-level of the main harmonic of a periodic analog signal. This work represents the main precursor of our approach to signal characterization. In fact, as it will be demonstrated later, the work in [87] can be reduced to a particular case of our characterization methodology. For this reason, let us detail briefly its functionality. Figure 4.4 depicts the block

FIGURE 4.4. Block diagram of the work in [87] for sinewave signal characterization

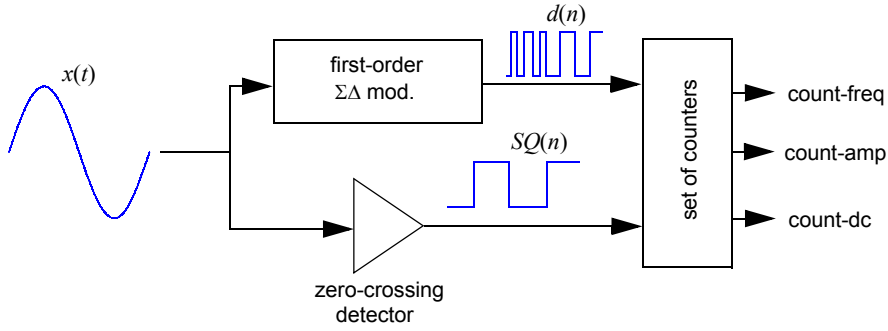


diagram of this approach. The basis of the procedure can be briefly explained as follows. The input signal  $x(t)$  is fed to a zero-crossing detector and to a 1st-order  $\Sigma\Delta$ -modulator. They generate a two-bit vector stream  $[d(n), SQ(n)]$ , where  $d(n)$  is the output of the modulator and  $SQ(n)$  the output of the zero-crossing detector. Such vector stream is processed between two positive (or negative) edges of  $SQ(n)$ , by a set of counters to extract a digitally encoded measurement (labelled *count-freq*, *count-amp* and *count-dc* in Figure 4.4) of the targeted parameters in the terms described below,

$$\text{count-freq} = \sum \left( \begin{array}{c} \text{number of clock cycles} \\ \text{in a period of } SQ(n) \end{array} \right) = \quad (4.1)$$

$$N \in \left[ \frac{T}{T_s} - 1, \frac{T}{T_s} + 1 \right]$$

$$\text{count-amp} = \sum_{n=1}^N [d(n)SQ(n)] \in \left[ \frac{2A}{\pi}N - 4, \frac{2A}{\pi}N + 4 \right] \quad (4.2)$$

$$\text{count-dc} = \sum_{n=1}^N d(n) \in [BN - 2, BN + 2] \quad (4.3)$$

where  $A$ ,  $B$  and  $T$  are the amplitude, DC-level and period of the input signal, respectively, normalized with respect to the full-scale range of the modulator, and  $T_s$  is the sampling period in the modulator.

The accuracy of the measurements in this approach is mainly determined by the oversampling ratio and the quantization error, which introduces the bounded terms ( $\pm 2$ ,  $\pm 4$ ). These errors may be

reduced to  $\pm 1$  by additional processing [87], and better results can be obtained by extending the measurement over a large number of periods and taking the mean value, but it is important to notice that it is not possible to reduce the relative error in the measurements by extending the number of periods of evaluation, since both the measurement and the error terms scale in the same way.

Although this basic approach has important properties in terms of simplicity, low overhead and robustness, it has some limitations. On the one hand, it requires the square-wave to be in phase with the main harmonic of the input signal and to have a duty cycle very close to the 50%. This restricts its application to low DC-level shifted signals as the square-wave is defined by the zero crossing points of the input signal, otherwise, it demands the introduction of a DC-insensitive comparator for this purpose. On the other hand, it can be demonstrated that odd harmonic components may affect the measurement of the amplitude if they are not small enough, and thus, the validity of the approach is restricted to low distorted signals, and only the main harmonic component can be characterized. The accuracy of the measurements is mainly limited by the oversampling ratio of the modulator, and hence, this need of oversampling may limit also its application in terms of frequency.

### 4.3. Proposed approach

The proposed methodology for the evaluation of periodic signals is an improved and generalized version of the work in [87]. This new evaluation strategy overcomes the limitations of [87] and also extends its functionality to the characterization of the signal harmonic components, both magnitude and phase. Furthermore, the accuracy of the measurements is greatly improved.

As pointed before, any digital scheme for the characterization of analog signals has to take into account two main factors: the analog to digital conversion scheme, and the processing of the resulting digitally encoded signal. Both points will be considered separately in the next sections. Firstly, the theoretical basis of the proposed processing algorithm will be discussed. And afterward, we will focus on the choice and implementation of an A/D interface suitable for the efficient development of the proposed algorithm.

#### A. Theoretical basis

Let  $x(t)$  be a periodic signal with period  $T$  and square-integrable over the interval  $[0, T)$ . Such a signal can be expanded in its Fourier series expansion [88],[89] as,

$$x(t) = a_0 + \sum_{k=1}^{\infty} [a_k \cos(k\omega t) + b_k \sin(k\omega t)] \quad (4.4)$$

where  $\omega=2\pi/T$ , and the coefficients  $a_0$ ,  $a_k$ , and  $b_k$ , for any non-negative integer  $k$ , are,

$$a_0 = \frac{1}{T} \int_0^T x(t) dt \quad (4.5)$$

$$a_k = \frac{2}{T} \int_0^T x(t) \cos(k\omega t) dt \quad (4.6)$$

$$b_k = \frac{2}{T} \int_0^T x(t) \sin(k\omega t) dt \quad (4.7)$$

Thus, any periodic signal of period  $T$  is fully characterized by the set of its expansion coefficients  $\{a_0, a_k, b_k\}$ . Equation (4.4) can be rewritten as,



$$x(t) = B + \sum_{k=1}^{\infty} A_k \sin(k\omega t + \varphi_k) \quad (4.8)$$

where  $x(t)$  is described in terms of a sum of harmonic components with amplitudes  $A_k$ , phase shifts  $\varphi_k$ , and a DC level  $B$ . This set of parameters are related to the Fourier coefficients by,

$$\begin{aligned} a_0 &= B \\ a_k &= A_k \sin \varphi_k \\ b_k &= A_k \cos \varphi_k \end{aligned} \quad (4.9)$$

It is clear that the set of parameters  $\{B, A_k, \varphi_k\}$  also characterizes signal  $x(t)$ . However, the direct computation of  $\{a_0, a_k, b_k\}$  or  $\{B, A_k, \varphi_k\}$  according to their definitions is not practical for on-chip implementation: both sets of parameters require the computation of (4.5), (4.6), and (4.7), that is, signal  $x(t)$  has to be modulated by the sine and cosine eigenfunctions and integrated. Performing these operations on-chip is a challenging and resource-consuming task, what makes it unsuitable for its direct implementation within a BIST scheme. Instead of that, we propose an approximation of equations (4.5)-(4.7) that, as it will be demonstrated, will lead to an efficient and accurate methodology for on-chip characterization of periodic analog signals of known period. Our proposal is based on two main points: the definition of two signatures, based on square-wave modulation, that can be related to the Fourier coefficients, and the particularization of the general expansion (4.4) to the case of discrete-time signals. Square-wave modulation can be easily and inexpensively performed on-chip, while the discretization of the signal is in fact imposed by the unavoidable A/D interface before the processing algorithm. Figure 4.5 shows a conceptual comparison between the standard Fourier transform and our proposed approach. It is important to notice that in the scheme in Figure 4.5b the A/D conversion can be performed either before or after the multipliers.

**FIGURE 4.5. Conceptual block diagrams: a) Fourier transform; b) Proposed approach**

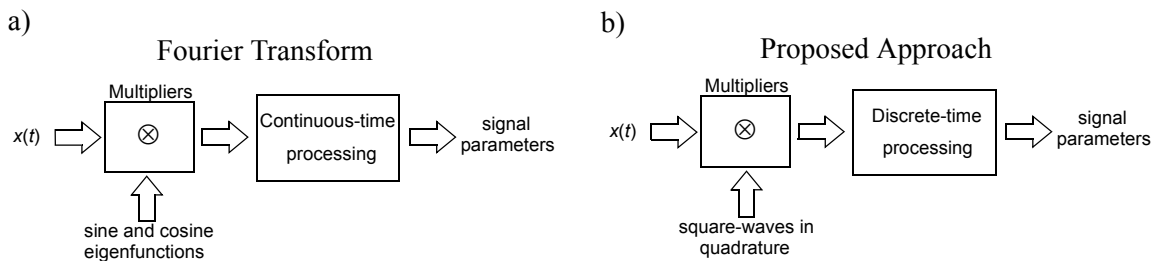
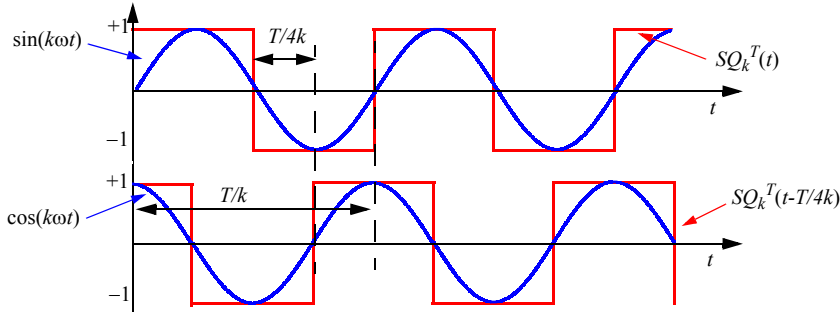


FIGURE 4.6. Square-wave signals as an alternative to sine and cosine eigenfunctions



In the following, we are going to analytically discuss the effects of these two points over the Fourier expansion.

*First point: Square-wave modulation*

This point consists of replacing the sine and cosine modulating signals by the modulation by two square-waves in quadrature:

$$\begin{aligned} \sin(k\omega t) &\leftrightarrow SQ_k^T(t) \\ \cos(k\omega t) &\leftrightarrow SQ_k^T\left(t - \frac{T}{4k}\right) \end{aligned} \quad (4.10)$$

where signal  $SQ_k^T(t)$  is a square-wave signal of period  $T/k$  and amplitude 1 (see Figure 4.6). Two signatures  $\hat{I}_{1k}$  and  $\hat{I}_{2k}$  are then defined as,

$$\begin{aligned} \hat{I}_{1k} &= \frac{1}{T} \int_0^T x(t) SQ_k^T(t) dt \quad k = 0, 1, 2, \dots \\ \hat{I}_{2k} &= \frac{1}{T} \int_0^T x(t) SQ_k^T\left(t - \frac{T}{4k}\right) dt \quad k = 0, 1, 2, \dots \end{aligned} \quad (4.11)$$

That is, signatures  $\hat{I}_{1k}$  and  $\hat{I}_{2k}$  are the continuous integration of  $x(t)$  modulated by the square-waves in quadrature  $SQ_k^T(t)$  and  $SQ_k^T\left(t - \frac{T}{4k}\right)$ , respectively, along a whole period of the signal  $x(t)$ .

For the case  $k=0$ , it is assumed to be  $SQ_k^T(t) = SQ_k^T\left(t - \frac{T}{4k}\right) = 1$ .

If the expansion in (4.8) is introduced in the signature definitions (4.11), it is easy to obtain the expressions (see Appendix 3),

$$\hat{I}_{1k} = \frac{2}{\pi} \left( A_k \cos \varphi_k + \sum_{i=1}^{\infty} \frac{A_{(2i+1)k}}{(2i+1)} \cos \varphi_{(2i+1)k} \right) = \frac{2}{\pi} \left( b_k + \sum_{i=1}^{\infty} \frac{b_{(2i+1)k}}{2i+1} \right) \quad k = 1, 2, \dots, \quad (4.12)$$

$$\hat{I}_{2k} = \frac{2}{\pi} \left( A_k \sin \varphi_k + \sum_{i=1}^{\infty} \frac{A_{(2i+1)k}}{(2i+1)} \sin \varphi_{(2i+1)k} \right) = \frac{2}{\pi} \left( a_k + \sum_{i=1}^{\infty} \frac{a_{(2i+1)k}}{2i+1} \right) \quad k = 1, 2, \dots, \quad (4.13)$$

$$\hat{I}_{10} = \hat{I}_{20} = B = a_0 \quad (4.14)$$

As it can be seen in these expressions, signatures  $\hat{I}_{1k}$  and  $\hat{I}_{2k}$  (for  $k \neq 0$ ) are composed by two components: a first one proportional to the Fourier expansion coefficients  $b_k$  and  $a_k$ , respectively, and a second component proportional to a linear combination of the Fourier coefficients at odd multiples of the  $k$ -th expansion frequency.

If  $x(t)$  is a band-limited signal (as it is the usual case in most practical situations) then the number of harmonic components is limited (namely  $L$  harmonic components) and equations (4.12) and (4.13) can be easily simplified,

$$\begin{aligned} \hat{I}_{1k} &= \frac{2}{\pi} \left( A_k \cos \varphi_k + \sum_{i=1}^L \frac{A_{(2i+1)k}}{(2i+1)} \cos \varphi_{(2i+1)k} \right) = \frac{2}{\pi} \left( b_k + \sum_{i=1}^L \frac{b_{(2i+1)k}}{2i+1} \right) \\ \hat{I}_{2k} &= \frac{2}{\pi} \left( A_k \sin \varphi_k + \sum_{i=1}^L \frac{A_{(2i+1)k}}{(2i+1)} \sin \varphi_{(2i+1)k} \right) = \frac{2}{\pi} \left( a_k + \sum_{i=1}^L \frac{a_{(2i+1)k}}{2i+1} \right) \end{aligned} \quad (4.15)$$

for  $k = 1, 2, \dots, L$

Given the set of signatures  $\hat{I}_{1k}$  and  $\hat{I}_{2k}$ , the expressions in (4.15) define a system of equations with  $2L$  equations and  $2L$  unknown variables ( $A_k$  and  $\varphi_k$ , for  $k=1, 2, \dots, L$ ) that can be solved to obtain the signal parameters  $A_k$  and  $\varphi_k$  from the signatures  $\hat{I}_{1k}$  and  $\hat{I}_{2k}$ . In other words, if  $x(t)$  is a band-limited square-integrable periodic signal, then the set of signatures  $\hat{I}_{1k}$  and  $\hat{I}_{2k}$ , defined as (4.11), fully

characterizes signal  $x(t)$ . For instance, Table 4.1 shows the obtained signatures for different values of  $k$  and  $L=4$ .

**TABLE 4.1. Results of both signatures  $\hat{I}_{1k}$  and  $\hat{I}_{2k}$  for different values of  $k$  and  $L=4$ .**

$k$	$\hat{I}_{1k}$	$\hat{I}_{2k}$
0	$B$	$B$
1	$\frac{2}{\pi} \left[ A_1 \cos \varphi_1 + \frac{A_3}{3} \cos \varphi_3 \right]$	$\frac{2}{\pi} \left[ A_1 \sin \varphi_1 + \frac{A_3}{3} \sin \varphi_3 \right]$
2	$\frac{2}{\pi} A_2 \cos \varphi_2$	$\frac{2}{\pi} A_2 \sin \varphi_2$
3	$\frac{2}{\pi} A_3 \cos \varphi_3$	$\frac{2}{\pi} A_3 \sin \varphi_3$
4	$\frac{2}{\pi} A_4 \cos \varphi_4$	$\frac{2}{\pi} A_4 \sin \varphi_4$

From these signature values, it is straightforward to deduce that the characteristic parameters of  $x(t)$  can be extracted as follows,

$$B = \hat{I}_{10} = \hat{I}_{20} \quad (4.16)$$

$$A_k^2 = \left( \frac{\pi}{2} \right)^2 [(\hat{I}_{1k})^2 + (\hat{I}_{2k})^2] \quad k = 1, \dots, 4 \quad (4.17)$$

$$\tan \varphi_k = \frac{\hat{I}_{2k}}{\hat{I}_{1k}} \quad k = 1, \dots, 4 \quad (4.18)$$

where it has been assumed that  $A_1 \gg \frac{A_3}{3}$ . However, if this approximation does not hold, the contribution of  $A_3$  and  $\varphi_3$  in  $k=1$  can be subtracted, as they are isolated for  $k=3$ .

Notice that if  $SQ_k^T(t)$  is in phase with the corresponding  $k$ -th harmonic component, that is, if  $\varphi_k$  is zero, then there would be neither need to compute  $\hat{I}_{2k}$  nor the squaring operation to obtain the

amplitudes. However, this possibility is not practical, since the phase of the harmonic components, in general, cannot be known a priori.

Summarizing, it has been demonstrated that the set of signatures  $\hat{I}_{1k}$  and  $\hat{I}_{2k}$  can be used to fully characterize a periodic signal with a limited number of significant harmonic components in terms of its DC level and the amplitude and phase of its harmonic components.

*Second point: Particularizing to discrete-time signals*

The processing will be done in the digital domain, and therefore, after a discretization of the signal. The second consideration that we are going to introduce takes advantage of this discretization. Starting from the already defined signatures  $\hat{I}_{1k}$  and  $\hat{I}_{2k}$ , let us consider the case in which the signal to be characterized,  $x_{sh}(t)$ , is a sampled and held version of the original signal  $x(t)$ , as depicted in Figure 4.7.

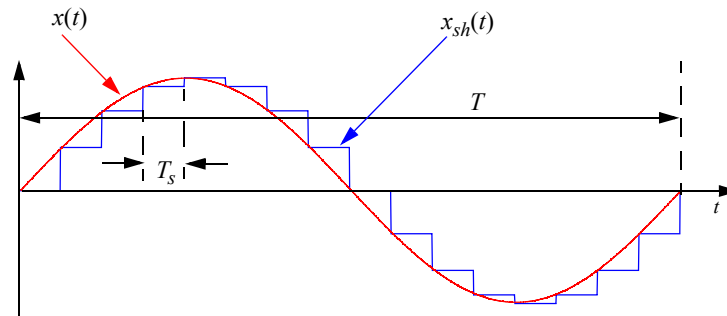
If the oversampling ratio defined as  $N=T/T_s$  is an integer number, where  $T$  is the period of signal  $x(t)$  and  $T_s$  is the sampling period, then  $x_{sh}(t)$  is also a periodic signal of period  $T$  and can be represented in the interval  $[0, T)$  as,

$$\begin{aligned} x_{sh}(t) &= x(nT_s) \quad \text{for } nT_s \leq t < (n+1)T_s \\ n &= 0, 1, 2, \dots, N-1 \end{aligned} \quad (4.19)$$

If  $N$  is a multiple of  $2^3k$  to ensure coherence between the signal and the modulation square waves (in the following, we will say two periodic signals to be coherent when the ratio of their respective periods is an integer number), the signature definitions can then be rewritten as,

$$\hat{I}_{1k} = \frac{1}{T} \int_0^T x_{sh}(t) S Q_k^T(t) dt = \frac{1}{N} \sum_{n=0}^{N-1} x(nT_s) S Q_k^T(nT_s) \quad k = 1, 2, \dots \quad (4.20)$$

**FIGURE 4.7. Sampled and hold signal**



$$\hat{I}_{2k} = \frac{1}{T} \int_0^T x_{sh}(t) S Q_k^T \left( t - \frac{T}{4k} \right) dt = \frac{1}{N} \sum_{n=0}^{N-1} x(nT_s) S Q_k^T \left( nT_s - \frac{T}{4k} \right) \quad k = 1, 2, \dots \quad (4.21)$$

Given that function  $S Q_k^T(t)$  only has two possible values, +1 or -1, equations (4.20) and (4.21) mean that signatures  $\hat{I}_{1k}$  and  $\hat{I}_{2k}$  in this particular case can be computed simply by adding and subtracting the signal samples according to the modulating square waves. For instance, for  $k=1$  equations (4.20) and (4.21) reduce to,

$$\begin{aligned} \hat{I}_{11} &= \frac{1}{N} \left[ \sum_{n=0}^{\frac{N-1}{2}} x(nT_s) - \sum_{n=\frac{N-1}{2}+1}^{N-1} x(nT_s) \right] \\ \hat{I}_{21} &= \frac{1}{N} \left[ \sum_{n=0}^{\frac{N-1}{4}} x(nT_s) - \sum_{n=\frac{N-1}{4}+1}^{\frac{3(N-1)}{2}} x(nT_s) + \sum_{n=\frac{3(N-1)}{2}+1}^{N-1} x(nT_s) \right] \end{aligned} \quad (4.22)$$

and similar expressions can be derived for each value of  $k$ .

The continuous integrals in the definition of the signatures are then simplified in this particular case to discrete summatories over the signal samples. The obtained signatures can then be used to compute the harmonic components of signal  $x_{sh}(t)$  applying the expressions (4.16)-(4.18) in the conditions previously discussed. But, since  $x_{sh}(t)$  is a sampled and held version of signal  $x(t)$ , then there is a direct relation between the spectral components of both signals. Indeed, the spectral components of signal  $x_{sh}(t)$  are the same that of signal  $x(t)$ , but modulated by a sampling function, and replicated around multiples of the sampling frequency. That is, if  $A_k$  denotes the amplitude of the  $k$ -th harmonic component of  $x(t)$  then the amplitude of the  $k$ -th harmonic component of  $x_{sh}(t)$  will be  $A_k |S_a(k\pi/N)|$ , where  $S_a(x)$  represents the sampling function. In any case, taking into account the contribution of the sampling, the  $A_k$  values can be recovered. In addition, if  $N$  is high enough, then it is verified that,

$$\lim_{N \rightarrow \infty} \left[ A_k \cdot \left| S_a \left( \frac{k\pi}{N} \right) \right| \right] = A_k, \quad (4.23)$$

that is, the contribution of the sampling disappears for large values of  $N$ .

Summarizing, it can be concluded that the spectral components of signal  $x(t)$  can be evaluated using the discrete integration method in (4.20) and (4.21), simply adding and subtracting the values of its samples  $x(nT_s)$ , with an error that goes to zero for large values of  $N$ , and that, in any case, can be taking into account computing a sampling function. In the following,  $N$  will be assumed to be large for simplicity.

### *B. A/D interface: exploiting the noise-shaping characteristics of a 1st-order $\Sigma\Delta$ modulator*

The mathematical results given in the previous section can be exploited to build an efficient system able to characterize periodic analog signals. According to (4.20) and (4.21), the resources needed to compute the signatures  $\hat{I}_{1k}$  and  $\hat{I}_{2k}$  of a periodic signal  $x(t)$  are reduced to the square-wave modulation and posterior integration of a sampled and held version of the signal to be evaluated.

It should be clear by now that performing the integration of the samples in the analog domain is a challenging and resource consuming task. It is clearly more advantageous to perform this operation after an analog to digital conversion of the signal. Before proposing any particular implementation, the A/D interface must be carefully chosen. Introducing a full A/D converter may be troublesome for BIST applications. Instead of that, we propose the use of a first-order  $\Sigma\Delta$ -modulator with a 1-bit quantizer instead of a complete A/D interface to carry out a basic yet robust and simple A/D conversion. Figure 4.8 shows a general block diagram of a discrete-time first-order 1-bit  $\Sigma\Delta$ -modulator [47]. It is composed by a discrete integrator followed by a 1-bit quantizer. In order to analyze this modulation scheme with the purpose of adapting it to our characterization algorithm, let us consider the  $\Sigma\Delta$ -modulator model depicted in Figure 4.9. In what follows, and without loss of generality, the full scale of the modulator will be assumed to be 1, and hence any other signals will be normalized with respect to the full scale.

**FIGURE 4.8. First-order  $\Sigma\Delta$  modulator block diagram**

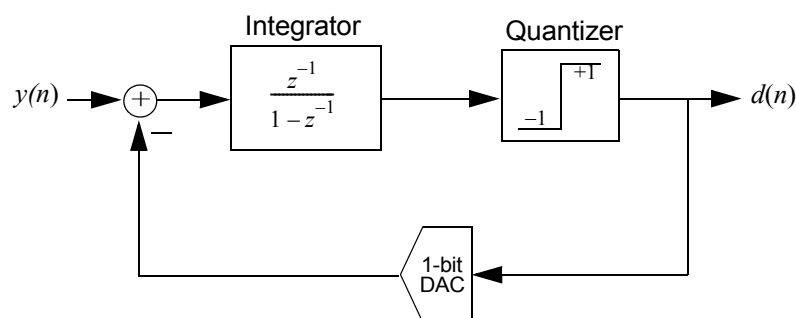
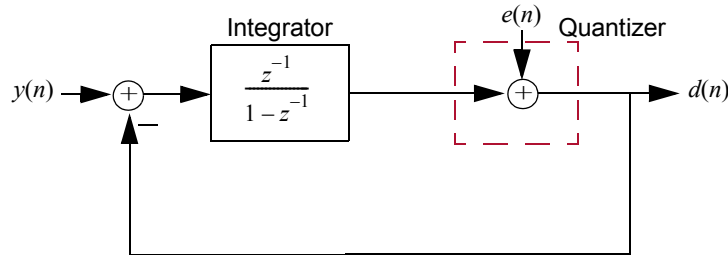


FIGURE 4.9. First-order  $\Sigma\Delta$  modulator model

The response  $d(n)$  at the output of the modulator in Figure 4.9 can be expressed as a function of the input  $y(n)$  and the quantization error  $e(n)$  as,

$$d(n) = y(n-1) + \{e(n) - e(n-1)\} \quad (4.24)$$

where  $y(n) = y(nT_s)$ , and  $T_s$  is the sampling period. As equation (4.24) shows, the input signal simply passes through the modulator with a delay, while the quantization noise is differentiated.

At this point, let us remember that our processing algorithm is based on the discrete integration of a sampled and square-wave modulated signal. Let us show what happens if the  $\Sigma\Delta$ -modulator output is integrated. Starting from equation (4.24), the discrete integration of the bit stream over a number  $P$  of samples is given by,

$$\sum_{n=1}^P d(n) = \sum_{n=1}^P y(n) + \sum_{n=1}^P \{e(n) - e(n-1)\} = \sum_{n=0}^{P-1} y(n) + \{e(P) - e(0)\} \quad (4.25)$$

That is, the direct integration of the bit-stream  $d(n)$  at the output of the modulator represents a measurement of the discrete integration of its input signal  $y(n)$ , and cancels the contribution of the quantization errors, with the exception of the error terms corresponding to the first and last samples. This is a very desirable feature for our characterization scheme. Indeed, assuming that there is no over-range in the modulator, then the quantization error  $e(n)$  verifies

$$e(n) \in [-1, 1], \quad (4.26)$$

that is, the quantization error introduces an uncertainty  $\varepsilon = e(P) - e(0)$  of  $\pm 2$  in the discrete integration (4.25), as it can be estimated by



$$\{e(P) - e(0)\} \leq |e(P) - e(0)| \leq 2 \quad (4.27)$$

so it can be concluded that,

$$\sum_{n=1}^P d(n) \in \left[ -2 + \sum_{n=0}^{P-1} y(n), 2 + \sum_{n=0}^{P-1} y(n) \right] \quad (4.28)$$

Equation (4.28) means that the discrete integration of the input signal  $y(n)$  can be computed by performing the direct integration of the bit-stream  $d(n)$  with a bounded error that, in any case, is limited to  $\pm 2$ . In addition, this error term does not scale with the number of samples, so if  $N$  is the oversampling ratio in the  $\Sigma\Delta$ -modulator and the integration is extended to an integer number  $M$  of periods of  $y(n)$ , then the total number of samples to which the integration is extended will be  $P=MN$ , while the error term keeps bounded. This means that the relative error of the computed integration will then be decreased in the said factor  $M$  with respect to the integration over a single period.

The use of first-order  $\Sigma\Delta$  modulation instead of a full A/D conversion not only simplifies the A/D interface, but also it has been demonstrated that exploiting the noise-shaping characteristics of this modulation scheme we can achieve a significant improvement in the accuracy of the measurements, since the quantization errors naturally compensate themselves in the integration. In addition, this integration of the bit-stream can be directly implemented using simple digital counters, which simplifies the implementation of the digital circuitry.

#### *Putting together the square-wave modulation and the $\Sigma\Delta$ modulation*

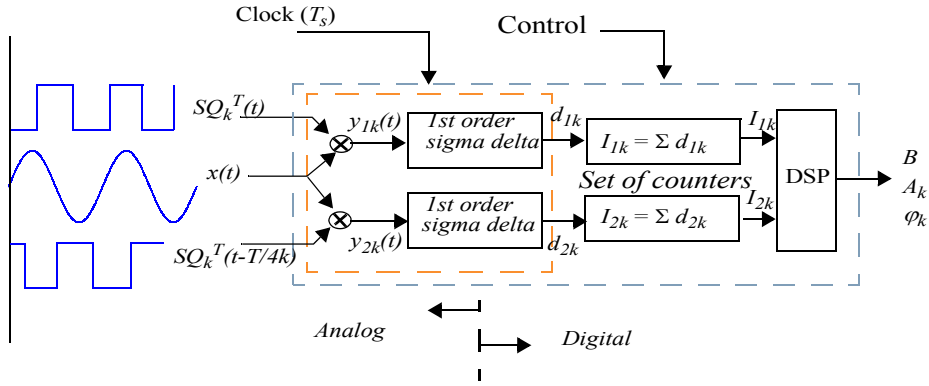
Once that we have selected the first-order  $\Sigma\Delta$  modulation as A/D interface, the only factor that we still have to deal with for the implementation of the proposed characterization scheme is the required square-wave modulation. Two possibilities arise: modulating the input signal in the analog domain, before the  $\Sigma\Delta$  modulation, or modulating the output of the  $\Sigma\Delta$ -modulator in the digital domain, just before the integration. Let us analyze both possibilities separately.

##### *a. Input square-wave modulation in the analog domain*

Figure 4.10 shows the block diagram of an implementation of the proposed signal characterization scheme which makes use of input square-wave modulation. Let us analyze the functionality of this system.

In this implementation, the signal under evaluation  $x(t)$ , with period  $T$ , is firstly modulated in the analog domain by the two square waves in quadrature  $SQ_k^T(t)$  and  $SQ_k^T\left(t - \frac{T}{4k}\right)$ . The resulting signals, labelled  $y_{1k}(t)$  and  $y_{2k}(t)$ , are fed into two matched 1st-order  $\Sigma\Delta$ -modulators. The oversampling ratio in the modulators is fixed to  $N=T/T_s$ , where  $T_s$  is the sampling period. The

**FIGURE 4.10. Implementation of the proposed signal characterization scheme: input square-wave modulation**



generated bit-streams  $d_{1k}(n)$  and  $d_{2k}(n)$  are then integrated using a set of counters along an integer number  $M$  of periods of the signal under evaluation. This way, signatures  $I_{1k}$  and  $I_{2k}$  are obtained. These signatures can be expressed as,

$$I_{1k} = \sum_{n=1}^{MN} d_{1k}(n) \quad ; \quad I_{2k} = \sum_{n=1}^{MN} d_{2k}(n) \quad (4.29)$$

It has been demonstrated already that the discrete integration of the modulator output is a measurement of the discrete integration of its input signal, but with a bounded error term due to the quantization error (see (4.28)). Then, it can be assured that,

$$I_{1k} = \sum_{n=1}^{MN} d_{1k}(n) \in \left[ -2 + \sum_{n=0}^{MN-1} y_{1k}(n), 2 + \sum_{n=0}^{MN-1} y_{1k}(n) \right] \quad (4.30)$$

$$I_{2k} = \sum_{n=1}^{MN} d_{2k}(n) \in \left[ -2 + \sum_{n=0}^{MN-1} y_{2k}(n), 2 + \sum_{n=0}^{MN-1} y_{2k}(n) \right]$$

Signals  $y_{1k}(t)$  and  $y_{2k}(t)$  are the results of the square-wave modulation of the input signal  $x(t)$ . If the oversampling ratio  $N$  is an integer multiple of  $2^3k$  to ensure coherence between the input signal  $x(t)$  and the modulating square-waves in quadrature, then equation (4.30) can be rewritten as,

$$\begin{aligned}
I_{1k} &\in \left[ -2 + \sum_{n=0}^{MN-1} x(nT_s)SQ_k^T(nT_s), 2 + \sum_{n=0}^{MN-1} x(nT_s)SQ_k^T(nT_s) \right] \\
I_{2k} &\in \left[ -2 + \sum_{n=0}^{MN-1} x(nT_s)SQ_k^T\left(nT_s - \frac{T}{4k}\right), 2 + \sum_{n=0}^{MN-1} x(nT_s)SQ_k^T\left(nT_s - \frac{T}{4k}\right) \right]
\end{aligned} \tag{4.31}$$

The obtained expressions for signatures  $I_{1k}$  and  $I_{2k}$  in equation (4.31) are formally identical to the signatures  $\hat{I}_{1k}$  and  $\hat{I}_{2k}$  in (4.20) and (4.21), respectively, with the exception of the error terms  $+2$  and  $-2$ , and the normalization factor  $1/N$ . That is, equation (4.31) can be rewritten as a function of signatures  $\hat{I}_{1k}$  and  $\hat{I}_{2k}$  as,

$$I_{1k} \in [MNI_{1k}^{\hat{}} - 2, MNI_{1k}^{\hat{}} + 2] \quad ; \quad I_{2k} \in [MNI_{2k}^{\hat{}} - 2, MNI_{2k}^{\hat{}} + 2] \tag{4.32}$$

For instance, Table 4.2 shows the expected signatures  $I_{1k}$  and  $I_{2k}$  at the output of the counters in Figure 4.10 for each harmonic  $k$  as a function of the oversampling ratio in the modulator,  $N$ , and the number of periods to which the integration is extended,  $M$  (in the sake of simplicity it has been assumed that  $x(t)$  has only four significant harmonic components, and that the oversampling ratio  $N$  is high enough to neglect the correction of the sampling function). (Let us remember that all the magnitudes are normalized with respect to the full scale range of the modulator.)

**TABLE 4.2. Signature results for the scheme in Figure 4.10 for four harmonic components.**

$k$	$I_{1k}$	$I_{2k}$
0	$MNB \pm 2$	$MNB \pm 2$
1	$\frac{2MN}{\pi} \left( A_1 \cos \varphi_1 + \frac{A_3}{3} \cos \varphi_3 \right) \pm 2$	$\frac{2MN}{\pi} \left( A_1 \sin \varphi_1 + \frac{A_3}{3} \sin \varphi_3 \right) \pm 2$
2	$\frac{2MN}{\pi} A_2 \cos \varphi_2 \pm 2$	$\frac{2MN}{\pi} A_2 \sin \varphi_2 \pm 2$
3	$\frac{2MN}{\pi} A_3 \cos \varphi_3 \pm 2$	$\frac{2MN}{\pi} A_3 \sin \varphi_3 \pm 2$
4	$\frac{2MN}{\pi} A_4 \cos \varphi_4 \pm 2$	$\frac{2MN}{\pi} A_4 \sin \varphi_4 \pm 2$

As it can be seen, Table 4.2 is formally similar to Table 4.1 except for the bounded errors  $\pm 2$ . It is worth to notice that signatures  $I_{1k}$  and  $I_{2k}$ , due to their definitions (4.29), are always integer numbers inside the extreme values defined by the error terms  $\pm 2$ . The targeted signal parameters, that is, harmonic amplitudes, phase shifts, and DC-level, can be estimated as suggested in the previous section within the limits imposed by the bounded error terms associated to the signatures. Thus, it can be ensured that,

$$B \in \frac{1}{MN} [\min(I_{10} + \varepsilon_{10}), \max(I_{10} + \varepsilon_{10})] \quad \text{or} \quad (4.33)$$

$$\frac{1}{MN} [\min(I_{20} + \varepsilon_{20}), \max(I_{20} + \varepsilon_{20})]$$

$$(A_k)^2 \in \left( \frac{\pi}{2MN} \right)^2 \left[ \begin{array}{l} \min \{ (I_{1k} + \varepsilon_{1k})^2 + (I_{2k} + \varepsilon_{2k})^2 \}, \\ \max \{ (I_{1k} + \varepsilon_{1k})^2 + (I_{2k} + \varepsilon_{2k})^2 \} \end{array} \right] \quad (4.34)$$

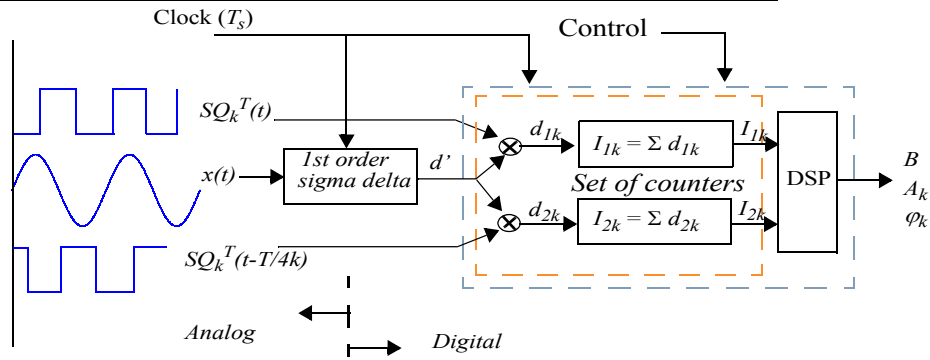
$$\tan \varphi_k \in \left[ \min \left( \frac{I_{2k} + \varepsilon_{2k}}{I_{1k} + \varepsilon_{1k}} \right), \max \left( \frac{I_{2k} + \varepsilon_{2k}}{I_{1k} + \varepsilon_{1k}} \right) \right] \quad (4.35)$$

where it has been assumed  $\frac{2MNA_3}{3\pi} < 1$ . In fact, given an  $A_3/A_1$  ratio,  $M$  and  $N$  can be selected to assure that assumption, while keeping a good accuracy in the measurement of  $A_1$ . Otherwise, it should be necessary to take into account the contribution of  $A_3$  and  $\varphi_3$  into the computation of  $A_1$  and  $\varphi_1$ , as they are isolated for  $k=3$ . The coefficients  $\varepsilon_{1k}$ ,  $\varepsilon_{2k}$  ( $k=0, 1, 2, \dots$ ) are the unknown error terms limited to  $\varepsilon_{1k}, \varepsilon_{2k} \in [-2, 2]$ . It is worth to remark that the error terms do not scale with the number of integration samples, while signatures  $I_{1k}$  and  $I_{2k}$  are directly proportional to the number of samples. This result is very important, because it means that the relative error of the measurements can be reduced simply by increasing the total number of samples,  $MN$ , to which the integration is extended.

#### *b. Digital square-wave modulation before the integration*

Let us consider now the possibility of introducing the square-wave modulation in the digital domain after the  $\Sigma\Delta$ -modulation. Figure 4.11 presents a block diagram of this alternative implementation. Formally, its functionality is similar to the one in Figure 4.10, but the digital bit-streams  $d_{1k}(n)$  and  $d_{2k}(n)$  are generated in a different way. In this case, the input signal  $x(t)$  is firstly modulated by a first-order  $\Sigma\Delta$ -modulator. The square-wave modulation is then applied in the digital

**FIGURE 4.11. Implementation of the proposed signal characterization scheme: digital square-wave modulation**



domain, to the bit-stream at the output of the modulator  $d'(n)$  to generate the two digital bit-streams  $d_{1k}(n)$  and  $d_{2k}(n)$ . The rest of the processing is similar to that in Figure 4.10.

The scheme in Figure 4.11 presents important advantages in terms of hardware and simplicity with respect to the implementation in Figure 4.10. Thus, only one  $\Sigma\Delta$ -modulator is required, and most of the processing is done in the digital domain. However, it suffers an important limitation in terms of accuracy. It can be justified as follows. Accordingly to the scheme in Figure 4.11 and equation (4.24), the error term introduced in the bit-stream  $d_{1k}(n)$  (a similar analysis can be done for  $d_{2k}(n)$ ) due to the quantization noise in the modulator is given by,

$$\varepsilon(n) = SQ_k^T(n) \{e(n) - e(n-1)\} \quad (4.36)$$

If  $\varepsilon(n)$  is integrated along  $M$  periods of the input signal (of period  $T=NT_s$ ), it gives,

$$\sum_{n=1}^{MN} \varepsilon(n) = \sum_{n=1}^{MN} SQ_k^T(n) \{e(n) - e(n-1)\} \in [-2(Mk+1), 2(Mk+1)] \quad (4.37)$$

Equation (4.37) means that the relative error in the signatures  $I_{1k}$  and  $I_{2k}$  in the scheme of Figure 4.11 is increased, with respect to the scheme in Figure 4.10, by a factor that is twice the index of the harmonic of interest multiplied by the number of periods  $M$  to which the integration is extended. So, the relative weight of the quantization error in the measurement of the targeted signal parameter is not reduced by increasing the number of periods taken into account, and even worse, the weight is increased by the index of the harmonic. In conclusion, the alternative scheme in

Figure 4.11 is in general not suitable for high accuracy applications unless the oversampling ratio in the  $\Sigma\Delta$ -modulator is extremely high.

Note also that the scheme in Figure 4.11 reduces to the scheme in [87] when the signal under evaluation is in phase with the modulating square-wave  $SQ_k^T(t)$ . In this case there would be no need to compute signature  $I_{2k}$ , however, in addition to its limitations in terms of accuracy, this approximation is not practical if this synchronization is not possible.

### C. High level validation using MATLAB

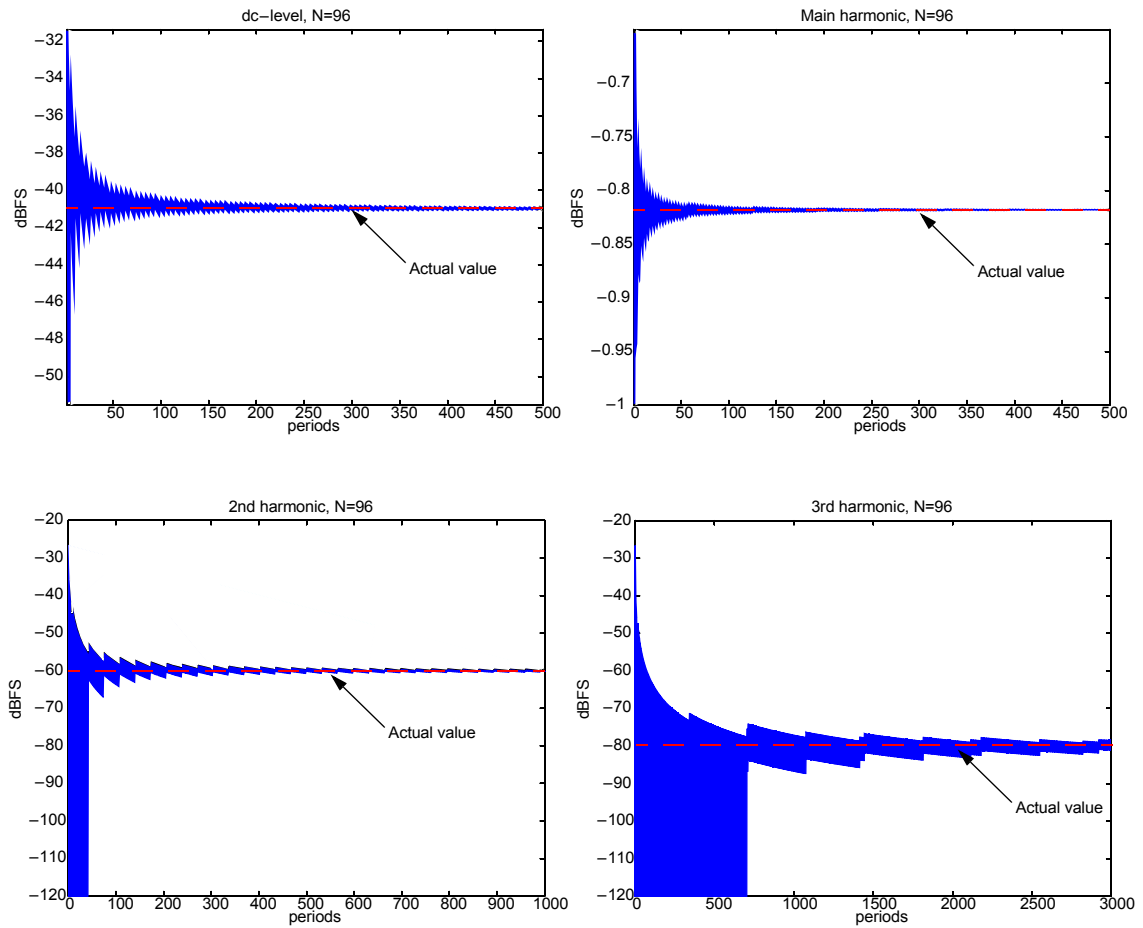
The feasibility of the proposed approach has been verified using behavioral simulations in SIMULINK/MATLAB. The signal analyzer depicted in Figure 4.10 has been implemented using a SIMULINK model for the 1st-order  $\Sigma\Delta$ -modulators, the counters, and the DSP block. The  $\Sigma\Delta$ -modulators have been modelled following the guidelines given in [90]. In this first validation, ideal modulators have been used. That is, in the modulator scheme in Figure 4.8 it has been considered that the functionality of the integrator, quantizer, and feedback D/A converter are ideal.

In order to provide an example of this validation, a signal containing three harmonic components and a DC level has been fed to the modelled system (see Table 4.3), and measurements of the magnitude of each component were performed. Figure 4.12 shows the evolution of the confidence intervals obtained in each measurement for an oversampling ratio  $N=96$  as a function of the number of periods,  $M$ , taken into account for each evaluation. The results agree perfectly with the expected ones, and show how the accuracy for a given magnitude increases with the number of periods taken for evaluation.

**TABLE 4.3. Signal components. Values in dBFS are normalized with respect to the full-scale range of the modulator ( $FS=1$ )**

Signal component	Actual value
DC level	-41.01 dBFS
Main harmonic magnitude, $A_1$	-0.82 dBFS
2nd harmonic magnitude, $A_2$	-60 dBFS
3rd harmonic magnitude, $A_3$	-80 dBFS
Phase-shifts, $\varphi_1$ , $\varphi_2$ , and $\varphi_3$	random

FIGURE 4.12. Confidence intervals versus number of periods taken for evaluation



The non-idealities of the building blocks that compose the proposed characterization system may limit the ideal behavior depicted in Figure 4.12. It should be clear that the most limiting block is the  $\Sigma\Delta$ -modulator. Although the study of most of the  $\Sigma\Delta$ -modulator non-idealities is specific of each particular design, some typical issues, such as the offset of its building blocks and the integrator leakage, can be discussed from a general point of view. In the following, the effects of offsets and leakage will be discussed, and in the next chapter, the other non-idealities of the building blocks will be considered over a particular design example.

### Offset

Up to now, the offsets of the different blocks composing the modulator have not been considered. The effect of the offset can be computed according to the linear model shown in Figure 4.13, where  $V_{offINT}$ ,  $V_{offQ}$ , and  $V_{offDAC}$  represents the offset of the integrator, quantizer, and D/A converter, respectively.

Thus, the output of the modulator,  $d(n)$ , can be written as a function of the input,  $y(n)$ , the quantization error,  $e(n)$ , and the offset of the different blocks,  $V_{offINT}$ ,  $V_{offQ}$ , and  $V_{offDAC}$ , as,

$$\begin{aligned} d(n) &= y(n-1) + V_{offINT}(n-1) - V_{offDAC}(n-1) + \\ &+ \{e(n) - e(n-1)\} + \{V_{offQ}(n) - V_{offQ}(n-1)\} = \\ &= y(n-1) + V_{offINT} - V_{offDAC} + \{e(n) - e(n-1)\} \end{aligned} \quad (4.38)$$

Equation (4.38) shows that the offsets associated to the integrator and to the D/A converter add to the input. Thus, it can be defined an input referred offset  $V_{off}$  as,

$$V_{off} = V_{offINT} - V_{offDAC}, \quad (4.39)$$

FIGURE 4.13.  $\Sigma\Delta$  modulator linear model including the offsets of the building blocks

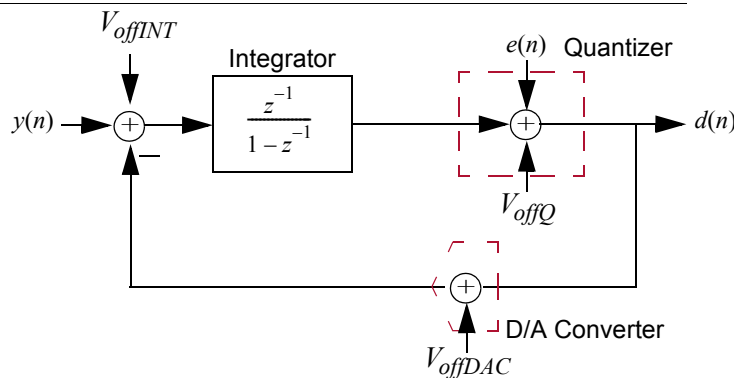
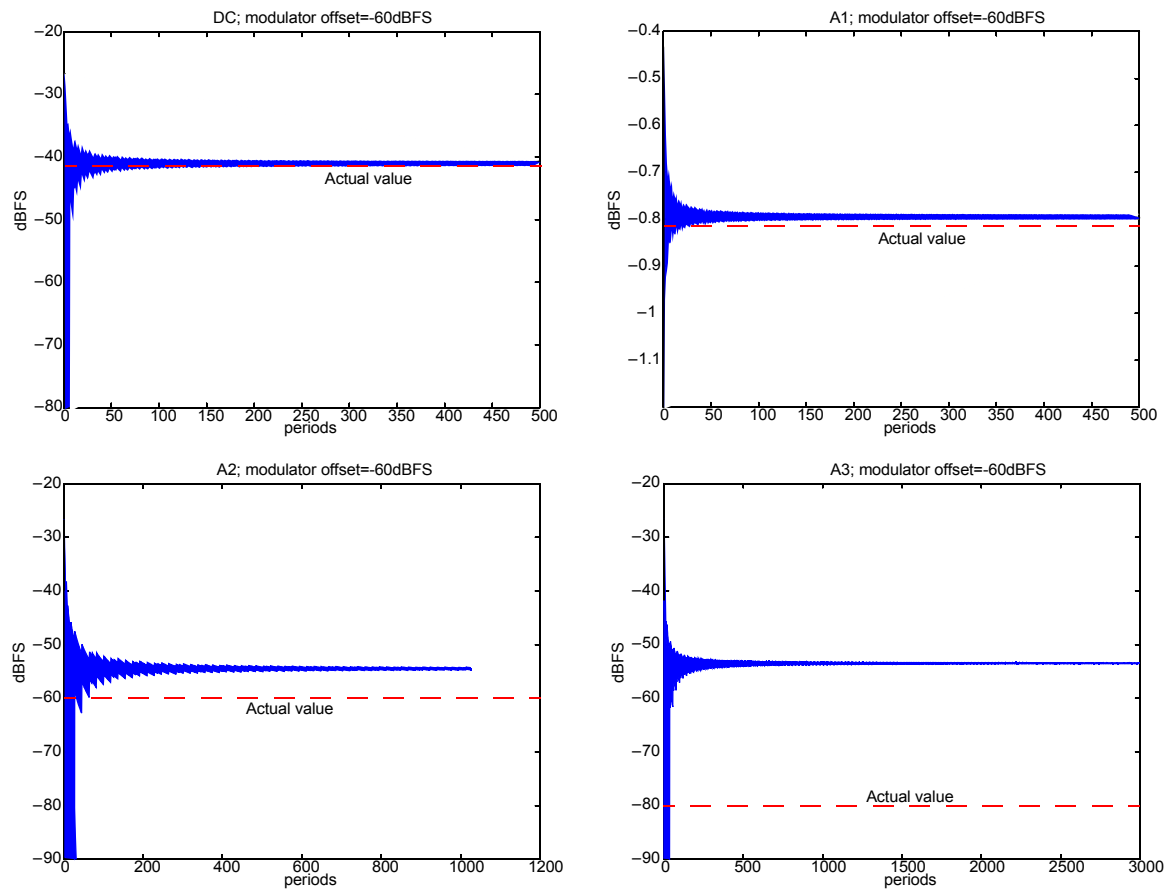




FIGURE 4.14. Effect of a  $-60\text{dBFS}$  modulator offset level in the measurements

which would corrupt the signatures  $I_{1k}$  and  $I_{2k}$  in a factor  $MNV_{off}$  since it is also integrated together with the modulated signals. If  $MNV_{off} \geq 1$ , it should be necessary to compensate it in order to maintain the accuracy of the measurements. Figure 4.14 shows high level simulations including an offset level of  $-60\text{dBFS}$ . It is clear to see the deviation in the measurements due to the offset.

At least two possibilities can be addressed to compensate the contribution of the offset in the measurements. One of them may consist of the correction of the signatures  $I_{1k}$  and  $I_{2k}$  through the previous measurement of  $V_{off}$ . Equation (4.25) suggest that it can be done by applying an input signal

$v(n)$  whose integration along a number  $S$  of samples is null, that is,  $\sum_{n=0}^{S-1} v(n) = 0$ . In this particular case, equation (4.25) reduces to,

$$\sum_{n=1}^S d(n) = SV_{off} + e(S) - e(0) \in [SV_{off} - 2, SV_{off} + 2] \quad (4.40)$$

So,  $V_{off}$  can be estimated with a relative accuracy of  $\pm 2/S$ . The contribution  $SV_{off}$  can then be extrapolated and subtracted from the signatures  $I_{1k}$  and  $I_{2k}$ . In principle, the most simple signal for this offset calibration would be  $v(n)=0$ , but this is not valid as a first-order  $\Sigma\Delta$ -modulator may have a limit cycle for DC inputs and thus, this approach may lead to wrong results. Instead of that, any periodic signal that is modulated by a square wave of frequency half of the signal can be used.

Another possibility exists at the expense of doubling the test time if the same accuracy wants to be maintained. The idea consists of changing the sign of the modulation square waves at the middle of the evaluation. The total number of evaluation periods should be even. A pair of signatures  $[I_\alpha, I_\beta]$  is obtained for each original signature  $I_{1k}$  and  $I_{2k}$ , where the first element,  $I_\alpha$ , corresponds to the integration over the first half of the evaluation and the second element,  $I_\beta$ , to the integration over the second half. In this way, as the offset of the modulator is not modulated, it is possible to compensate it by subtracting the two partial signatures  $I_\alpha$  and  $I_\beta$ . That is,

$$\begin{aligned} I_\alpha &= \sum_{n=1}^{S/2} d(n) = \frac{I}{2} + \frac{S}{2} V_{off} \pm 2 \\ I_\beta &= \sum_{n=S/2+1}^S d(n) = \frac{-I}{2} + \frac{S}{2} V_{off} \pm 2 \end{aligned} \quad (4.41)$$

where  $I$  is the signature  $I_{1k}$  or  $I_{2k}$  to be measured. So, subtracting  $I_\beta$  from  $I_\alpha$ ,

$$I_\alpha - I_\beta = I \pm 4 \quad (4.42)$$

As it can be deduced, the offset is compensated, but the quantization error is now double. It means that to maintain the accuracy in the measurement of  $I$  with respect to the quantization error, the number of evaluation periods must be doubled  $S \rightarrow 2S$ .

*Integrator leakage*

In the previous sections, the integrator in the  $\Sigma\Delta$ -modulator has been modelled by the  $z$ -domain transfer function  $H(z)$ ,

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \quad (4.43)$$

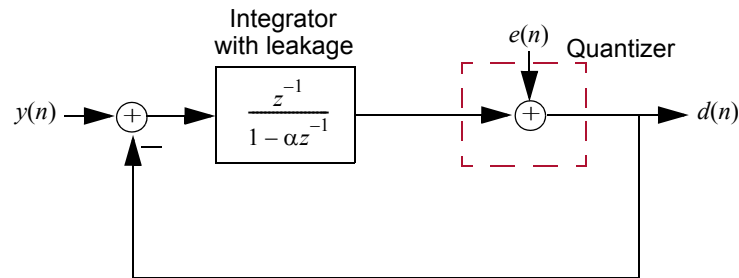
The DC gain of the integrator described by (4.43) is infinite. However, any practical integrator will have a finite gain limited by circuit constraints. The direct consequence of this integrator “leakage” is that only a fraction  $\alpha$  of the previous output of the integrator is added to each new input sample [91]. The transfer function of the integrator with leakage becomes,

$$H(z) = \frac{z^{-1}}{1 - \alpha z^{-1}} \quad (4.44)$$

The effect of this integrator leakage over the measurements can be analytically estimated from the linear model in Figure 4.15. It is easy to demonstrate that the integration over  $P$  samples of the modulator output, including the effect of the integrator leakage, is given by,

$$\sum_{n=1}^P d(n) = \frac{1}{1 - (\alpha - 1)} \left\{ \sum_{n=0}^{P-1} y(n) + (\alpha - 1)[d(0) - d(P)] - (\alpha - 1) \sum_{n=1}^P e(n) + \alpha[e(P) - e(0)] \right\} \quad (4.45)$$

**FIGURE 4.15.**  $\Sigma\Delta$  modulator linear model including the integrator leakage effect



As it can be deduced from (4.45), there is an error in the signal gain which translates directly to the integration of samples  $y(n)$ , but even worse, due to the leakage coefficient  $\alpha$ , error terms do not compensate in the integration as in the ideal case, and a new error term appears related to the first and last samples of signal  $d(n)$  during the integration. Signatures will then be corrupted by an error term  $\varepsilon$  that can be defined as,

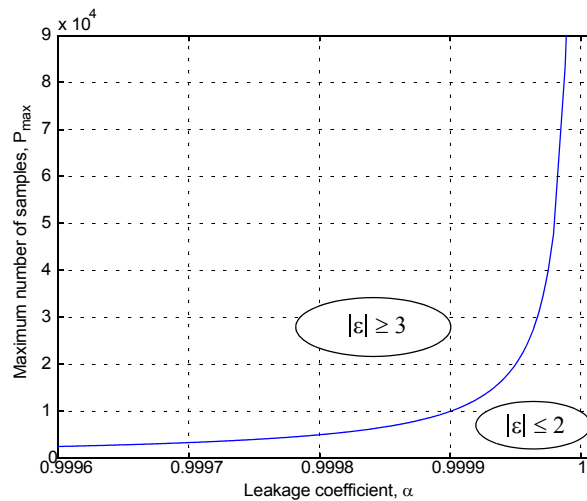
$$\varepsilon = \frac{1}{1 - (\alpha - 1)} \left\{ (\alpha - 1)[d(0) - d(P)] - (\alpha - 1) \sum_{n=1}^P e(n) + \alpha[e(P) - e(0)] \right\} \quad (4.46)$$

Assuming that there is no overrange in the modulator this error term can be estimated as,

$$|\varepsilon| \leq \frac{1}{1 + (1 - \alpha)} \{ (2 + P)(1 - \alpha) + 2\alpha \} \quad (4.47)$$

Note that, as expected, expressions (4.45) and (4.47) reduce to the ideal cases (4.25) and (4.27), respectively, as coefficient  $\alpha$  tends to unity. Equation (4.47) is important. It means that for each particular value of coefficient  $\alpha$ , there is a maximum value of samples  $P_{max}$  to which the integration can be extended without increasing the error term  $\varepsilon$  beyond the ideal  $\pm 2$ . Figure 4.16 shows this limit value  $P_{max}$  as a function of the leakage coefficient.

**FIGURE 4.16. Maximum number of samples to which the integration can be extended due to the integrator leakage**



**FIGURE 4.17. Effect of the integrator leakage in the measurement of the main harmonic component**

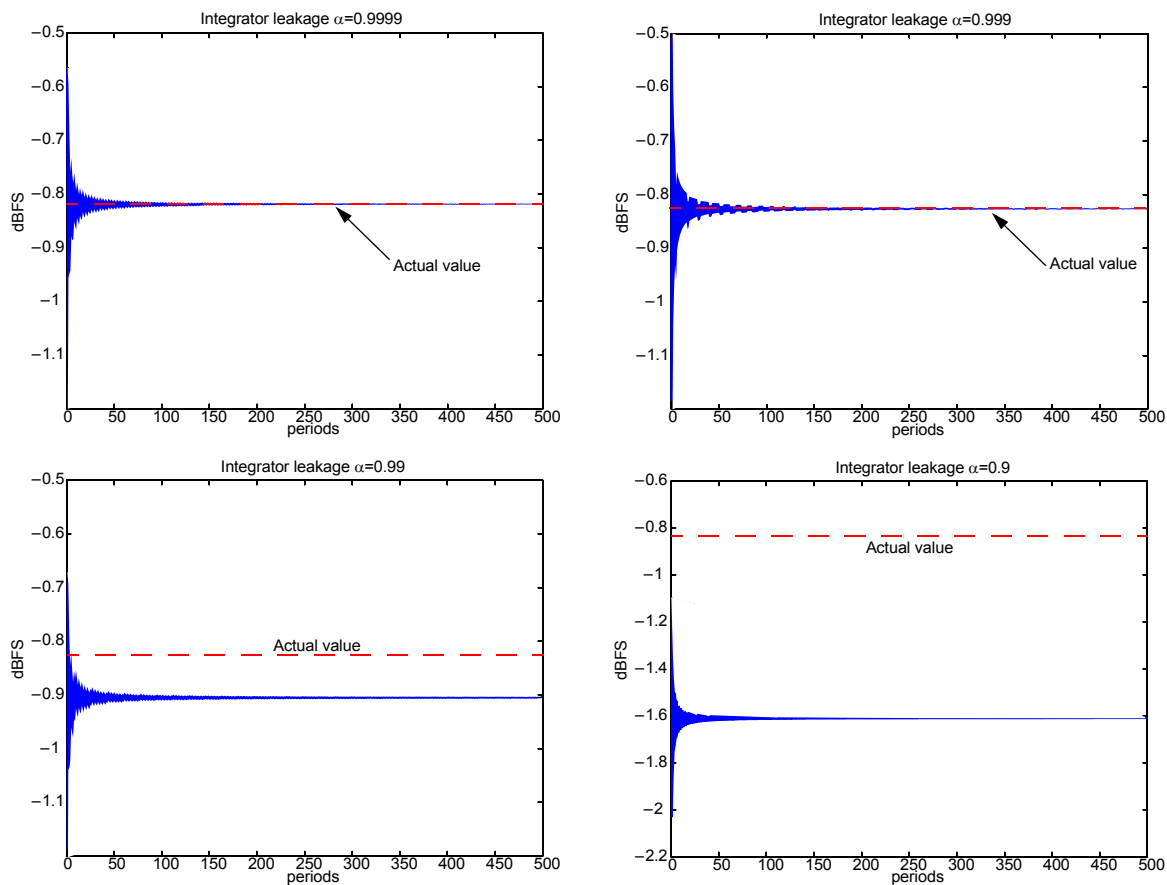


Figure 4.17 shows high level simulations for different values of coefficient  $\alpha$ . It is clear to see the deviation in the measurements due to the integrator leakage. Fortunately, values of  $\alpha$  very close to unity are feasible, as it will be detailed later over a particular design. Otherwise the effect of the integrator leakage would corrupt the measurement, as shown in Figure 4.17.

#### 4.4. General aspects about the practical implementation

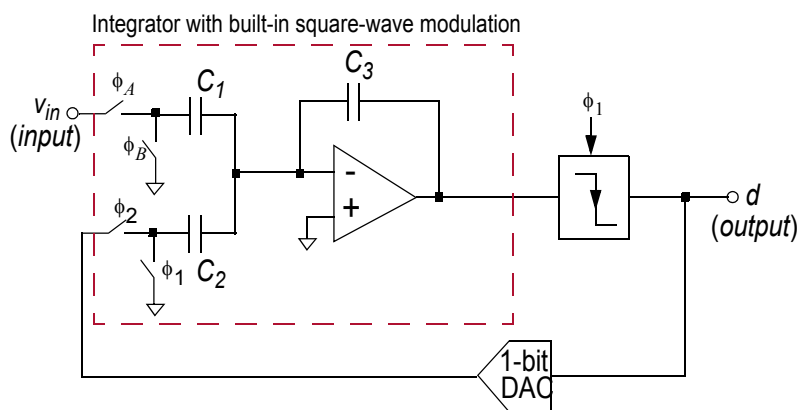
This section is dedicated to make some general considerations about the main blocks composing the proposed signal analyzer, namely the  $\Sigma\Delta$ -modulator and the DSP, and the generation and synchronization of the required clock and modulation square-waves. Additional considerations at a lower abstraction level will be given in the next chapter over a particular design example.

##### A. $\Sigma\Delta$ -modulator

The first-order  $\Sigma\Delta$ -modulator is the key block in the implementation of the proposed characterization scheme. Indeed, the performance of the modulator defines the performance of the proposed analyzer. In other words, it can be said that the application of the proposed analysis scheme is effectively limited to the range of application of this particular modulation strategy. In this sense, discrete-time  $\Sigma\Delta$ -modulators working in the range of tens of MHz have been reported [92]-[94], and state-of-the-art switched-capacitor circuits can work in the range of hundreds MHz clock frequency, what means that the present approach can be useful for the evaluation of signals in the range of tens of MHz while a reasonable oversampling ratio is maintained. A continuous-time implementation of the  $\Sigma\Delta$  modulator is also possible, and allows to extend the frequency range of application of the proposed approach to higher frequencies [95]-[96].

The proposed characterization strategy makes use of a square-wave modulation of the signal before the  $\Sigma\Delta$ -modulator. This square-wave modulation can be easily included at the input stage of the  $\Sigma\Delta$ -modulator. As an example, Figure 4.18 shows the block diagram of a switched-capacitor single-ended implementation of a first-order  $\Sigma\Delta$ -modulator with built-in square-wave modulation.

**FIGURE 4.18. Block diagram of a SC first-order  $\Sigma\Delta$ -modulator with built-in input square-wave modulation**



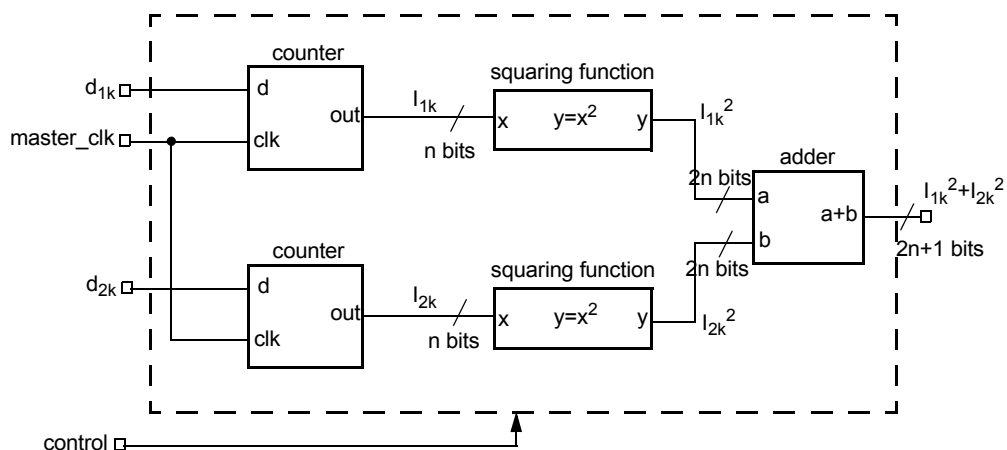
This modulator works with two non-overlapped clock phases  $\phi_1$  and  $\phi_2$ . However, switches connected to the input and controlled by  $\phi_A$  and  $\phi_B$  can be used to perform the modulation by the square-wave. It only requires to invert or not the contribution of the input,  $V_{in}$ , to the output,  $d$ , of the modulator. In this way, if  $\phi_A=\phi_2$  and  $\phi_B=\phi_1$  the integrator has an inverting input configuration with respect to  $V_{in}$ . On the contrary, if  $\phi_A=\phi_1$  and  $\phi_B=\phi_2$  the non-inverting input configuration is obtained.

### B. Digital Signal Processing (DSP) Block

Concerning the DSP, two counters are required for the computation of the digital signatures  $I_{1k}$  and  $I_{2k}$ , and two squaring functions together with a full-adder are required for the evaluation of the harmonic signatures  $(I_{1k})^2+(I_{2k})^2$ . Figure 4.19 shows a simplified block diagram of the proposed DSP block. Bit-streams  $d_{1k}(n)$  and  $d_{2k}(n)$  coming from the  $\Sigma\Delta$ -modulators are integrated using two digital counters. These counters perform a discrete integration of the signal, as it was discussed before. Basically, the state of each counter increments if its input is a logic ‘high’, while it decreases when its input is ‘low’. The results of this discrete integration, that is, digital signatures  $I_{1k}$  and  $I_{2k}$ , are then squared by the squaring function blocks and finally added to give the harmonic signature  $(I_{1k})^2+(I_{2k})^2$ .

An important point in this scheme is the computation of the squaring functions to obtain the final harmonic measurement. Notice that this function has only to be performed over a limited number of values ( $2L$  times for  $L$  harmonics), and can then be computed sequentially in several clock cycles to

FIGURE 4.19. DSP simplified block diagram



save area in an on-chip implementation. The main idea to evaluate sequentially the square of an  $n$ -bit binary-encoded integer number, is to break down the square into  $n$  additions, which can be evaluated in  $n$  clock cycles. Thus, let  $A_n = a_n a_{n-1} \dots a_2 a_1$  be a 2's complement encoded integer number. To evaluate  $A_n^2$  it is needed to compute,

$$\begin{array}{r}
 a_n a_{n-1} \dots a_2 a_1 \\
 \times \quad a_n a_{n-1} \dots a_2 a_1 \\
 \hline
 b_{1n} b_{1n-1} \dots b_{12} b_{11} \\
 b_{2n} b_{2n-1} \dots b_{22} b_{21} \\
 \dots \quad \dots \\
 b_{nn} b_{nn-1} \dots \quad b_{n1} \quad \dots \quad \dots \quad + \\
 \hline
 A_n^2 = c_{2n+1} c_{2n} \dots \dots \quad \dots \quad \dots \quad c_1
 \end{array} \tag{4.48}$$

where,

$$b_{ij} = \begin{cases} a_j & \text{if } a_i = 1 \\ 0 & \text{if } a_i = 0 \end{cases} \tag{4.49}$$

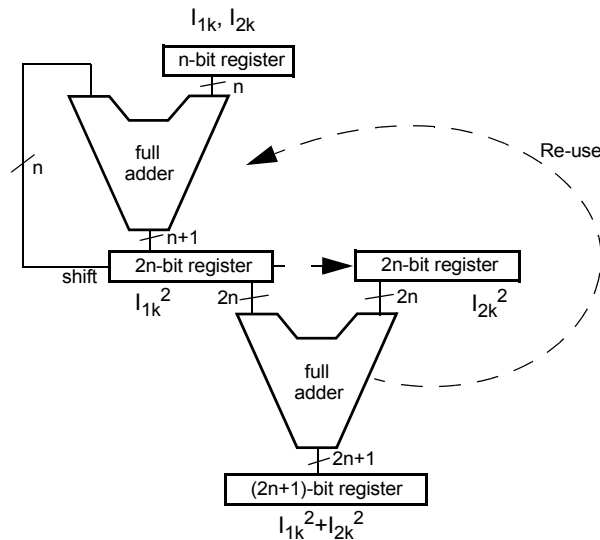
This way, the square can be evaluated sequentially, adding two rows each cycle, and requiring only a full adder and a shift register. It is important to notice that the encoding scheme of the counters should be able to work with positive and negative numbers. The choice of 2's complement encoding allows to simplify the design of the counters and adders since 2's complement numbers follow the same arithmetical rules than binary ones.

Figure 4.20 shows a possible implementation of the discussed sequential computation. It is possible to make a rough evaluation of the required resources for the case of sequential measurements.

The counter output  $I_{1k}$  is stored on an  $n$ -bit register. The value of  $n$  is determined by the expected values of the signatures. The squaring function can be realized using an  $n$ -bit full adder and a  $2n$ -bit register in  $n$  clock cycles. The result of this operation has to be stored for further processing, so another  $2n$ -bit register is needed. The squaring operation can be repeated for  $I_{2k}$  with the same hardware. Then the two square values has to be summed so a  $2n$ -bit full-adder and a  $(2n+1)$ -bit register are needed. Since a  $2n$ -bit full-adder is used to do the final summation, the  $n$ -bit full-adder can be also avoided. Therefore, the total hardware would consist of one  $2n$  full-adder, one  $(2n+1)$ -bit



FIGURE 4.20. Possible implementation of the harmonic signature computation



register, two  $2n$ -bit registers, and two  $n$ -bit registers. A non optimized implementation of a full adder would require 28 transistors per bit and the registers would require 6 transistor per bit. Hence, this amounts to  $74n$  transistors approximately, which in terms of equivalent 2-input nand gates and for 14-bit precision, is equivalent to 260 logic gates.

The total computation time for  $L$  harmonic components can be easily estimated. Regarding the scheme in Figure 4.10, the evaluation of the signatures  $I_{1k}$  and  $I_{2k}$  is performed in parallel by the two digital counters on-the-fly, as the counters are triggered directly by the digital bit-streams generated by the two  $\Sigma\Delta$ -modulators. Thus, if  $M$  is the number of evaluation periods and  $N$  is the oversampling ratio, it takes  $LMN$  clock cycles to compute the  $2L$  signatures  $I_{1k}$  and  $I_{2k}$  ( $k = 1, \dots, L$ ). The subsequential evaluation of the harmonic signatures, using the proposed sequential scheme, takes  $L(2n+1)$  clock cycles for  $n$ -bit counters.

For typical values of  $M$ ,  $N$ , and  $n$ , the time needed for the computation of the squares is negligible with respect to the evaluation of the single signatures, so the evaluation can be considered on-the-fly with a good approximation. Obviously, it is also possible to optimize the hardware and reduce the computation time, since the same precision may not be required for each harmonic.

Also notice that there is a hardware saving alternative to the scheme in Figure 4.10, at the cost of doubling the test time. The extraction of the signatures  $I_{1k}$  and  $I_{2k}$  can be realized sequentially instead of in parallel. If the measurements are realized sequentially, only one  $\Sigma\Delta$ -modulator and one counter are required (plus some memory to store each  $I_{1k}$  and  $I_{2k}$  value). Otherwise, if the

measurements are performed fully in parallel, a modulator and a counter are required per signature. Actually, a trade-off exists between test-time and area.

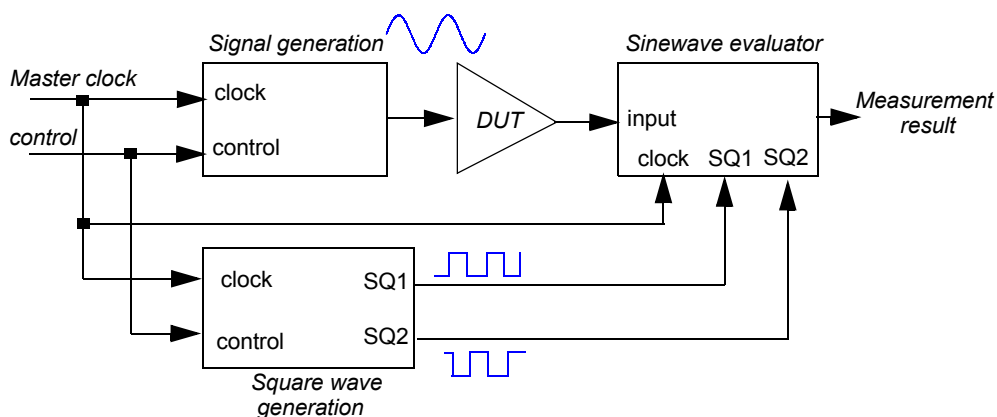
### C. Signal synchronization

The proposed method requires that the oversampling ratio of the  $\Sigma\Delta$ -modulator be an exact multiple of the factor  $2^3k$  where  $k$  refers to the index of the harmonic to be measured. In other words, coherence and synchronization between the signal to be evaluated and the sampling clock is needed. Obviously, in order to integrate the proposed strategy into a BIST scheme, the said requisites must be ensured.

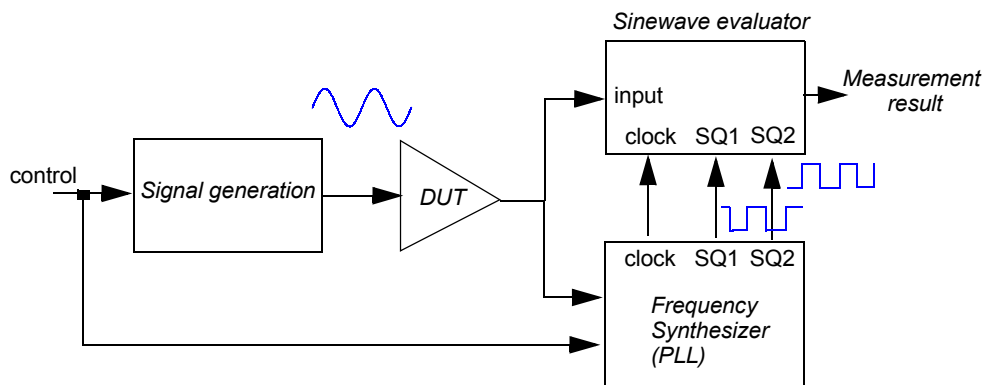
Sampling coherence and signal synchronization can be achieved by the scheme illustrated in Figure 4.21. The required signals are generated by a digitizer and square wave generators (shift registers) using the same master clock. This solution is appropriate when the test signals are generated off-chip by an ATE, or when the test stimulus generation core can be synchronized with the master clock. Several possibilities can be addressed in this line. For instance, the on-chip signal generators presented in [45],[52], and in this work in a previous chapter, are very suitable for this application, since the generated signal in these schemes is, by construction, synchronized with the master clock. The generation of the square waves in this case can be done easily from the master clock requiring only shift registers.

Another solution to accomplish the requisites of coherence and synchronization is based on the use of a PLL as shown in Figure 4.22. The idea is to capture the frequency of the signal,  $f_{in}$ , to be

FIGURE 4.21. Integration of the proposed sinewave evaluator in a BIST scheme using an external master clock



**FIGURE 4.22. Integration of the proposed sinewave evaluator in a BIST scheme using a frequency synthesizer (PLL)**

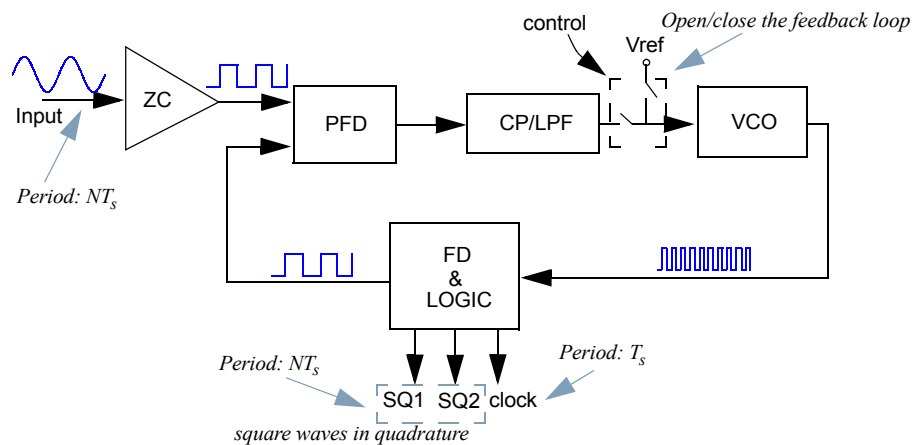


evaluated and generate a clock of frequency  $f_s$  accomplishing  $f_s/f_{in} \propto (2^3 k)$ . At the same time, the required square-waves can be straightforwardly derived through proper frequency division of the clock. In this way, the required oversampling ratio and the synchronization of the signals involved are ensured. Although the design of a PLL is in general a difficult task, the requisites for this application are very relaxed. For example, the PLL is used in this case as a frequency synthesizer, where jitter is not of main concern (the measurements are done taken into account a large number of samples), and the signal to be evaluated can be maintained stable while the measurement is performed, which facilitates the strategy for a fast acquisition and reduce the problems related to the lock range.

Figure 4.23 shows the block diagram of a typical PLL composed by a zero-crossing detector (ZC) to generate a squared-wave version of the input, a phase-frequency detector (PFD), a charge pump (CP), a lowpass filter (LPF), a voltage-controlled oscillator (VCO) and a frequency divider (FD). Both the sampling clock and the required square waves can be obtained easily from the FD.

One of the most critical blocks is the VCO, especially if it has to be tuned for a large range of frequencies. However, its design can be relaxed if we translate the tuning problem to the frequency divider, in such a way that the VCO is oscillating always at a frequency very close to a reference frequency (for that, the feedback loop is opened and the input of the VCO is set to a reference voltage  $V_{REF}$ ) while the divider is adjusted depending on the frequency of the input signal. It is translated to the evaluator measurement approach in terms of the oversampling ratio. For low frequencies the oversampling ratio can be made very high, thus reducing the number of periods that need to be taken into account for the measurement, and hence, the test time. On the other hand, if the

FIGURE 4.23. Block diagram of the proposed frequency synthesizer



input frequency is high, there is no matter if the oversampling ratio is reduced because the relative time consumed by a period is smaller.

But the above idea has also another important consequence. A control circuit can be added to open the feedback loop in order to detect which division of the reference frequency of the VCO is the closest to the frequency of the input signal. In this way, the feedback loop can be closed once the PLL is placed in a proper state that minimizes the capture time.

## 4.5. Summary

One of the key points in analog and mixed-signal testing is the characterization of analog periodic signals. Traditional test methods for analog and mixed-signal systems normally use periodic signals as test stimuli and apply complex processing algorithms to the response, usually in the digital domain (FFT, etc.), in order to extract the targeted test parameters. The complete and direct emulation of these traditional test methods for on-chip implementation and BIST applications are normally prohibitive due to the excessive overhead, except in very complex systems where the required hardware is already available on-chip.

This chapter presents a novel scheme for the evaluation of analog periodic signals. It is based on an approximation of the Fourier series expansion that can be very efficiently implemented on-chip. The proposed implementation is based on a double modulation, square-wave and sigma-delta, together with a very simple digital processing algorithm.

The proposed approach extracts, digitally encoded, the DC level and the amplitude and phase shifts of the harmonic components composing a periodic analog signal. The accuracy of the measurements is mainly determined by the product of the oversampling ratio in the  $\Sigma\Delta$ -modulator and the number of periods of the input signal taken for the evaluation. It restricts its actual use to signals from low to medium frequency range, up to tens of MHz, where the  $\Sigma\Delta$ -modulators can still work with reasonable oversampling ratios.

Some general implementation considerations have been provided while the simplicity and robustness of the required circuitry make the present approach very suitable for BIST applications, and also offers a great versatility in terms of programmability and synthesis.



## CHAPTER 5

**Practical Design of an Analog  
Periodic Signal Evaluator and  
Experimental Results**

*This chapter presents the design of an integrated prototype of the proposed signal analyzer, together with the discussion of the design methodology. The developed prototype has been integrated in a standard 0.35 $\mu$ m CMOS technology. Experimental measurements in the lab verify the feasibility of the approach and the functionality of the prototype.*

## 5.1. Introduction

In this chapter we are going to detail the design of the proposed scheme for the characterization of analog periodic signals. An integrated prototype has been developed in a standard  $0.35\mu\text{m}$ -3.3V CMOS technology as a vehicle to illustrate the design methodology and the feasibility of the approach. The design goal for the developed prototype will be a signal analyzer able to characterize signals in the range of audio.

In the following sections, the design of the prototype and its experimental characterization in the lab are detailed. This chapter is organized as follows. Firstly, Section 5.2 presents the design of the prototype, while Section 5.3 summarizes the main experimental results obtained in the lab. Finally, Section 5.4 remarks the main points of this chapter.

## 5.2. Prototype design

### 5.2.1. System level

The developed signal analyzer follows the scheme in Figure 4.10, which is reproduced here in Figure 5.1 for convenience. In this first prototype we have chosen to integrate the analog part of the analyzer, featuring the first-order  $\Sigma\Delta$ -modulators with built-in square-wave modulation, and to implement the digital part externally, using the processing capabilities of our test equipment. However, some design considerations for the digital part will also be given. In the following, the analog and the digital parts of the prototype will be discussed separately.

FIGURE 5.1. Block diagram of the proposed signal analyzer

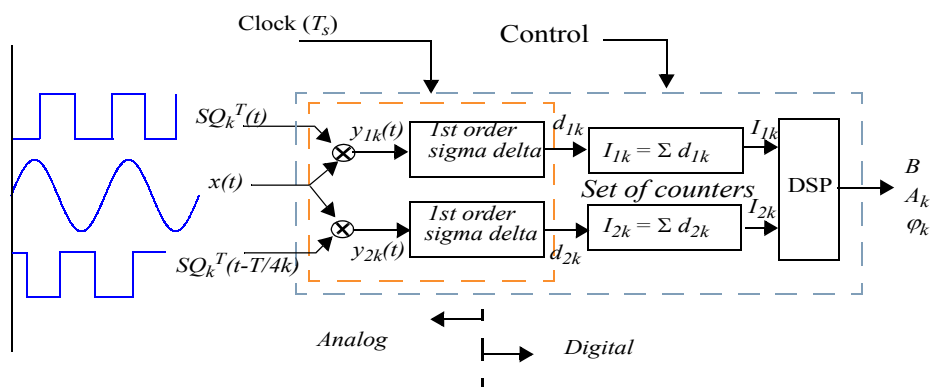
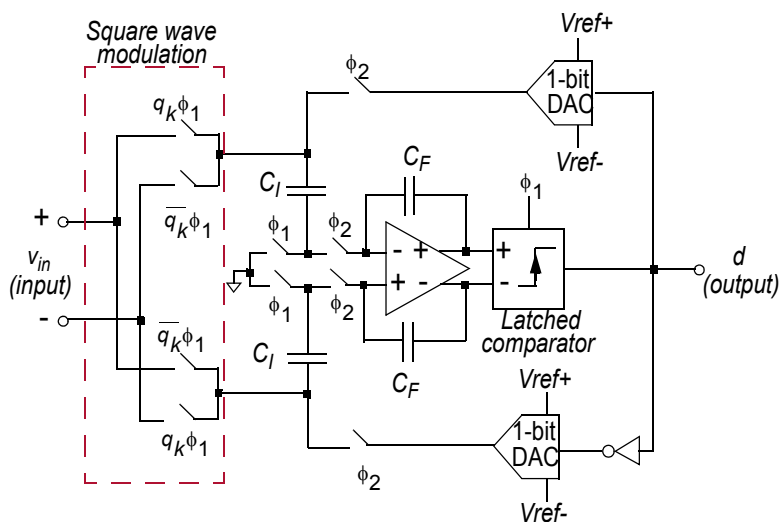




FIGURE 5.2.  $\Sigma\Delta$  modulator with built-in square-wave modulation



A. Analog Part:  $\Sigma\Delta$ -modulator with built-in input square-wave modulation

Concerning the modulator, some design considerations can be made. We have selected a typical fully-differential discrete-time implementation based on the switched-capacitor technique [97]. The block diagram of the selected modulator is shown in Figure 5.2. The modulator works with two non-overlapped clock phases  $\phi_1$  and  $\phi_2$ , and the required square-wave modulation has been implemented through a special input switching scheme. For keeping high enough oversampling ratios in the selected audio frequency range, the maximum sampling frequency is set to 2MHz approximately.

It should be clear that the most limiting block for the performance of the prototype is the modulator. Its performance is defined by its main building blocks, namely, the amplifier, and the comparator. Let us consider separately the characteristics of these building blocks.

- The amplifier

The most critical block in the design of the  $\Sigma\Delta$ -modulator is the amplifier. The performance of the amplifier in terms of DC gain, saturations, bandwidth, slew-rate, settling-time, etc. defines the performance of the modulator.

### Amplifier Gain (Integrator Leakage)

As discussed before, the finite amplifier gain deviate the integrator transfer function from the ideal case, causing that only a fraction  $\alpha$  of the previous output of the integrator is added to each new input sample. In this particular case, coefficient  $\alpha$  is given by

$$\alpha \cong 1 - \frac{C_I}{C_F A_0} \quad (5.1)$$

where  $A_0$  is the open-loop DC gain of the amplifier.

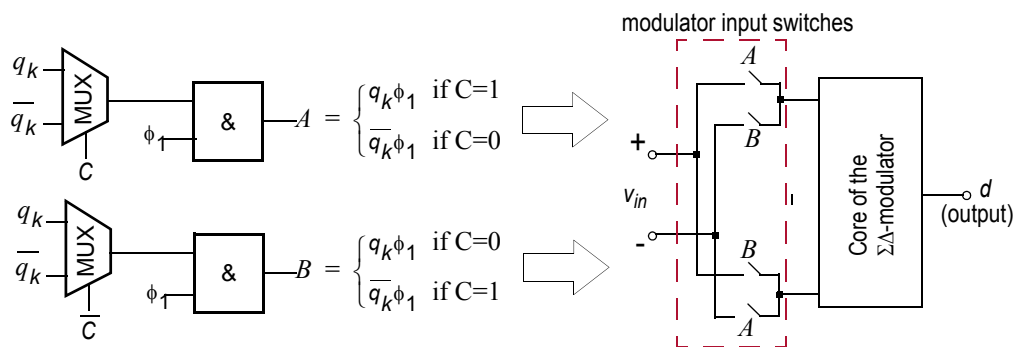
The DC gain of the amplifier has to be carefully chosen in order to maintain the error term (4.47) as close as possible to the ideal case ( $|\varepsilon| \leq 2$ ) in all the intended measurement range. Otherwise, as discussed previously, measurements will be corrupted by the integrator leakage. If the integrator gain,  $C_I/C_F$ , is set to 0.4, which limits the output swing of the amplifier to roughly 80% of the supply range to avoid saturation, then equation (5.1) can be used together with (4.47) to determine the adequate value of  $A_0$  for a specific application.

### Integrator offset

In the previous chapter it was demonstrated that the offset of the integrator, together with the D/A converter offset, contributes to a modulator offset that can corrupt the measurements. Two different methodologies were proposed to cancel the effect of the modulator offset in the measurements: one based on the direct measurement of this offset, and another one based on inverting the modulating square-waves. Let us present here a simple way to implement the second solution within the considered  $\Sigma\Delta$ -modulator, to make the measurements insensitive to the modulator offset.

The circuitry in Figure 5.3 has been included together with the  $\Sigma\Delta$ -modulator to add the desired capability to invert the modulating square-waves. This simple circuitry allows the inversion of the

**FIGURE 5.3. Generation of the input switches control signals for offset cancellation purposes**



input square-wave modulation when the control signal  $C$  changes its state. If signal  $C$  is changed at the middle of the evaluation time, this inversion can be used to compensate the effect of the modulator offset in the signatures, as explained in the previous chapter, by subtracting the two partial signatures obtained in each of the evaluation halves. Note also that this subtraction can be computed directly by the counters in the DSP if signal  $C$  is used also to invert their functionality at the middle of the evaluation. Control signal  $C$  can be generated together with the modulating square-waves adapting any of the proposed methods for the generation of the modulating square-waves addressed in the previous chapter.

#### *Amplifier Settling Time*

Assuming a dominant pole compensated amplifier, and in the case that the settling time is linear and not slew-rate limited, the change in the amplifier output can be modelled as,

$$v_{out} = V_o \left( 1 - e^{-\frac{t}{\tau}} \right) \quad (5.2)$$

where  $\tau$  is a time constant given by,

$$\tau = \frac{C_I + C_F}{2\pi \cdot GBW \cdot C_F}, \quad (5.3)$$

$GBW$  is the gain-bandwidth product of the amplifier, and  $V_o$  is the ideal output voltage.

Taking into account that in a first-order  $\Sigma\Delta$ -modulator the integrator is directly followed by a comparator, then it is not necessary to assure a complete settling of the signal at the output of the integrator, and the  $GBW$  specification can be relaxed. For instance, if the integrator gain,  $C_I/C_F$ , is set to 0.4, a good trade-off solution is to set the  $GBW$  to  $f_s/2$ , in such a way that the output at  $t = T_s/2$  will reach the 67% of its ideal final value  $V_o$ . Complete settling demands a higher gain-bandwidth product, larger than the sampling frequency. It must be noticed that the effect of incomplete settling degrades the  $SNR$  of the modulator, as it scales the signal but not the noise. Nevertheless, the proposed method averages the noise, so, in a first instance, an incomplete settling can be tolerated between reasonable limits.

#### *Amplifier Slew-Rate*

If the output of the amplifier is slew-rate limited the discussion above is not valid. The slewing will introduce distortion into the modulator output spectrum whether a comparator follows the integrator or not. This distortion must be avoided in order to properly measure the harmonic component of the input signal.

When the output of the modulator changes states, the output of the integrator changes by, at least,

$$\text{Minimum change in integrator output} = \frac{C_I FS}{C_F 2} \quad (5.4)$$

where  $FS$  is the full scale of the modulator.

If it is considered that the full evolution is slew-rate limited, then the minimum slew-rate of the amplifier can be estimated as,

$$SR = \frac{C_I}{C_F} FS \cdot f_s \quad (5.5)$$

However, larger changes at the output of the integrator are possible, also, the real evolution has always a linear settling part, and in practical applications, signal settling has to be usually reduced to a fraction of the clock phase duration. For these reasons, a more conservative limit for the slew-rate is necessary. Equation (5.5) should be seen as a minimum limit value to guide the design choice.

- *Comparator*

In general, the comparator is not as limiting as the amplifier for the performance of the modulator. Its performance in terms of gain and hysteresis has to be considered in the design of the modulator. As discussed before, the output of the integrator changes by at least (5.4) when the comparator changes states. If the hysteresis is less than this value and the gain of the comparator is high enough to make a full transition with this input difference, the modulator will function properly.

- *Mapping the specifications of the building blocks*

In the view of the previous analysis of the needed performance for each building block in the modulator, Table 5.1 shows the selected set of specifications for each block. Some considerations about these design choices can be made. Thus, the choice of the reference voltages for the feedback D/A converter defines a full-scale of 0.7V for the modulator, which corresponds to a differential input range of 1.4V. Concerning the amplifier, the selected 80dB DC gain, together with a 0.4 gain for the integrator, gives a value for the integrator leakage coefficient  $\alpha=0.99996$ , which according to (4.47) allows to extend the discrete integration of the signal to more than 25000 samples of the input signal without degrading the measurements. A conservative value has been chosen for the  $GBW$  and  $SR$  of the amplifiers to avoid incomplete settling and distortion of the signal. Concerning the comparator, according to the given design guidelines, it has to be able to resolve input differences of 140mV.

**TABLE 5.1. Selected specifications for the modulator building blocks**

<b>Integrator</b>	Gain, $C_I/C_F = 0.4$
<b>Amplifier</b>	DC gain = 80dB Gain-bandwidth product = 150MHz Slew-rate = 170V/ $\mu$ s
<b>Comparator</b>	Able to make a full transition with a 140mV input difference
<b>Feedback DAC reference voltages</b>	$V_{ref+} = 2V$ $V_{ref-} = 1.3V$

### *B. Digital part: DSP block*

The inherent simplicity of the DSP block discussed in the previous chapter opens the possibility of including it on-chip or implementing it directly in the ATE. The outputs of the  $\Sigma\Delta$ -modulators are two digital bit-streams that can be sent to the outside world for external processing. The processing is translated to the external equipment, but it has the advantage of low area overhead, since the analyzer is then reduced mainly to the  $\Sigma\Delta$ -modulators. If an on-chip implementation is chosen, such as the one proposed in Figure 4.19, then the key point in the design of the DSP is the sizing of the counters and registers. The length of the registers will limit the maximum number of samples that can be processed in the evaluation, and hence, will limit also the accuracy of the analysis. Thus, the sizing of the counters and registers should be carefully done according to the intended application.

It is worth noting that if in a particular application it is possible to synchronize the input signal and the modulating square-waves (or if the phase-shift between both signals can be estimated a priori) then it may be possible to minimize one of the counters, which can represent important savings in the total area overhead.

### *C. Validation of the specifications*

A validation of the selected set of specifications has been carried out through a behavioral model developed using Verilog-A. In order to be practical in the simulations, a realistic model for the  $\Sigma\Delta$ -modulator has been implemented following the modelling guidelines in [90]. Typical non-idealities common to SC circuits such as clock jitter and thermal noise have been also included in the model. The simulation conditions are listed in Table 5.2. A signal containing three harmonic components and a DC-level has been used as test input stimulus. Figure 5.4 shows the magnitude measurement histograms, obtained by performing 30 runs of each experiment, while Table 5.3 summarizes the

obtained confidence intervals for the magnitude of each signal component to show the precision of each measurement. Values in dBFS are normalized to the full-scale range of the modulator. The obtained results agree with the expected ones and, as it is shown, resolutions of fractions of dBFS are easily obtained.

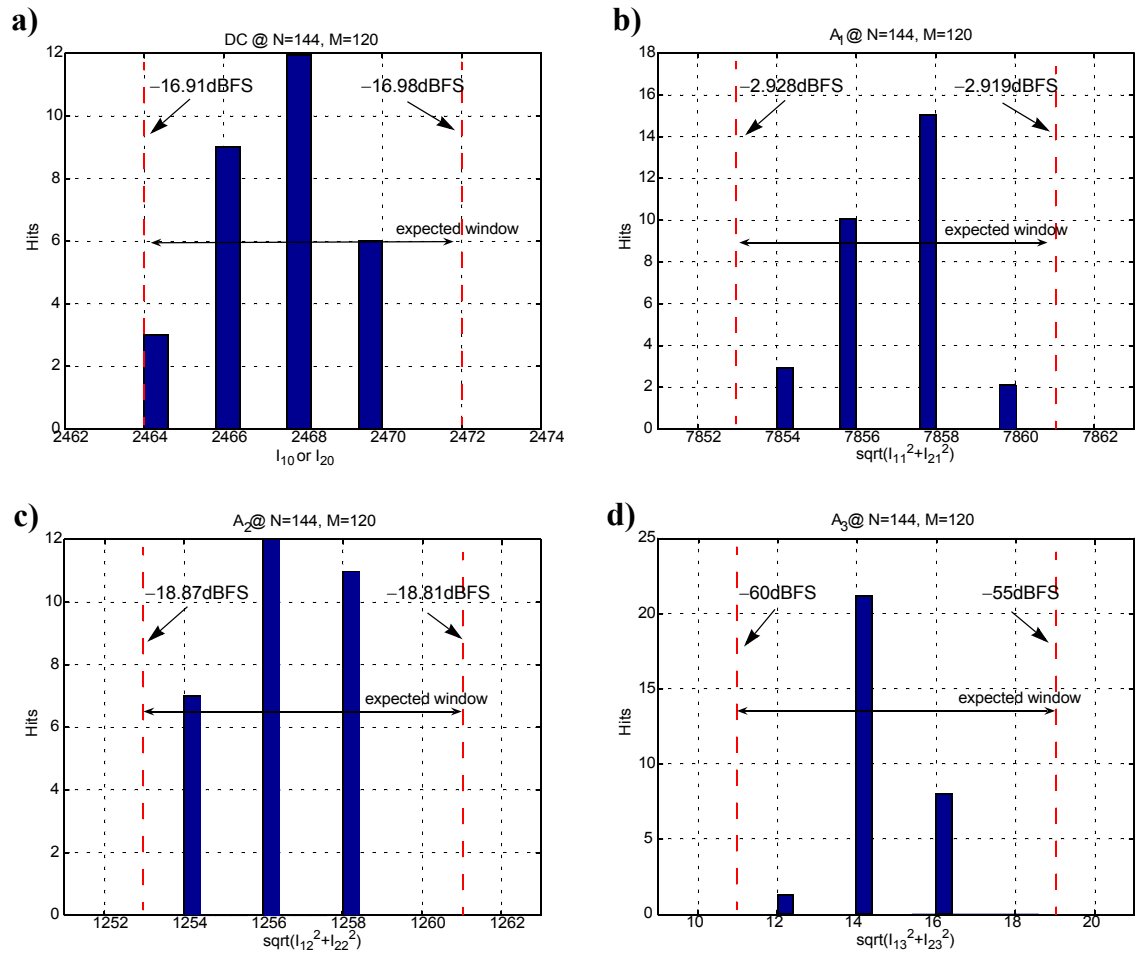
**TABLE 5.2. Simulation conditions**

<b>General conditions</b>	<b>modulator offset</b>	random (from $-10\text{mV}$ to $10\text{mV}$ )
	<b>Comparator hysteresis</b>	$6\text{mV}$
	<b>Temperature</b>	$300\text{K}$
	<b>Maximum clock jitter</b>	$1\text{ns}$
	<b>Oversampling ratio</b>	$144$
<b>Input stimulus</b>	<b>Frequency</b>	$8\text{kHz}$
	<b>DC level</b>	$100\text{mV}$
	<b>Main harmonic</b>	$A_1 = 500\text{mV}$
	<b>2nd harmonic</b>	$A_2 = 80\text{mV}$
	<b>3rd harmonic</b>	$A_3 = 1\text{mV}$

**TABLE 5.3. Expected intervals for each signal component. Values in dBFS normalized to the full-scale of the modulator**

<b>Component</b>	<b>Actual value (dBFS)</b>	<b>Obtained confidence interval (dBFS)</b>	<b>Number of evaluation periods</b>
DC	$-16.90$	$[-16.91, -16.89]$	120
$A_1$	$-2.923$	$[-2.928, -2.919]$	120
$A_2$	$-18.84$	$[-18.87, -18.81]$	120
$A_3$	$-57$	$[-60, -55]$	120

FIGURE 5.4. a) DC level measurements. b) Main harmonic measurements. c) 2nd harmonic measurements. c) 3rd harmonic measurements.



## 5.2.2. Building blocks design

### A. Analog part

#### The amplifier

The folded-cascode structure introduced in the previously discussed design of the discrete-time sinewave generator (see Chapter 3) has been chosen. Its main performance parameters, reproduced here in Table 5.4 for convenience, meet the selected amplifier specifications listed in Table 5.1, and are more than enough to handle signals in the frequency range of audio. The full schematic of the amplifier can be found in Figure 3.23 in Chapter 3. Reusing the design reduces significantly the design effort of the test core.

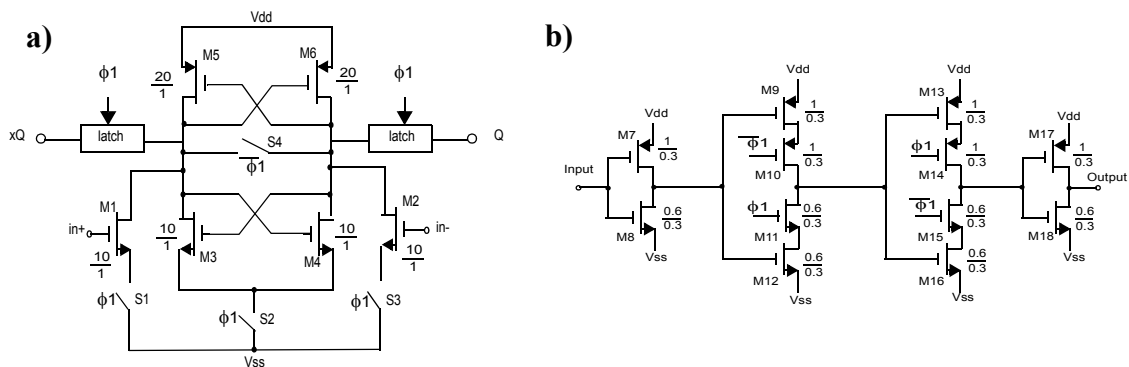
**TABLE 5.4. Amplifier performance parameters ( $V_{dd}=3.3V$ ,  $I_{bias}=60\mu A$ )**

<b>DC gain</b>	80dB
<b>Gain-bandwidth product</b>	180MHz
<b>Phase margin</b>	55°
<b>Settling time (1%)</b>	4.0ns
<b>Slew-rate</b>	170V/ $\mu s$

#### The latched comparator

A clocked comparator based on a dynamic latch (see Figure 5.5) has been selected [97]. It offers a good trade-off between simplicity and high speed. Transistors M3 to M6 compose a basic latch, while input transistors M1 and M2, that are in a common source amplifier configuration, unbalance

**FIGURE 5.5. a) Latched comparator schematic. b) Output latch**





the basic latch to enable the comparison of the input signals. These input transistors provide a moderate pre-amplification of the comparator input signal, and also reduces kickback noise issues [98]. Finally, a typical  $C^2$ MOS output stage latches the outputs of the comparator at the end of the  $\phi_1$  clock phase. Switch S4 erases the stored state of the latch before each comparison, while switches S1 to S3 reduce the power consumption cutting off the supply path in the resetting phase of the comparator. Transistor sizes  $W/L$  in Figure 5.5 are expressed in  $\mu\text{m}/\mu\text{m}$ .

#### *Feedback D/A converter*

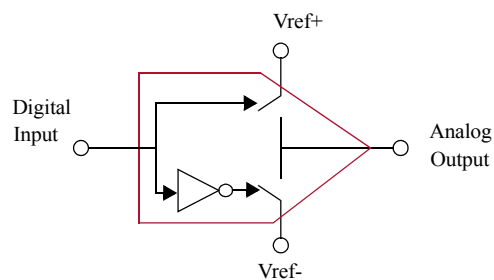
The 1-bit feedback D/A converters have been implemented by the simple scheme shown in Figure 5.6. It is based on CMOS switches connected to the analog reference voltages  $V_{ref+}$  and  $V_{ref-}$ .

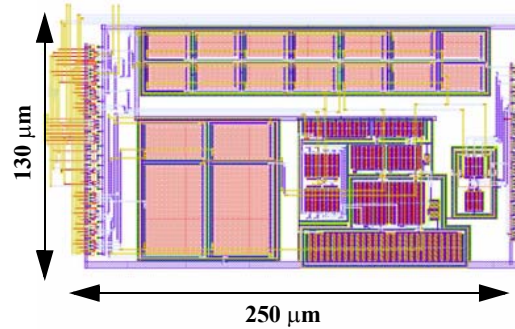
#### *Capacitors and switches*

The desired  $C_I/C_F$  ratio has been fixed to 0.4. In order to improve matching, capacitors  $C_I$  and  $C_F$  have been built using a common-centroid array of 14 polysilicon unit capacitors (7 for each signal path) of size  $10\mu\text{m}$  by  $10\mu\text{m}$  (about 211fF). Capacitor  $C_I$  is made from 2 unit capacitors and  $C_F$  from the other 5 in the array, which gives the desired  $2/5=0.4$  ratio.

Concerning the switches, minimum size CMOS complementary switches have been used to reduce feedthrough effects and maximize the dynamic range in the modulator.

**FIGURE 5.6. 1-bit feedback D/A converter**



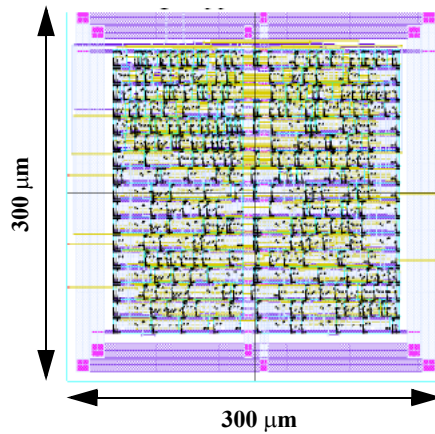
**FIGURE 5.7. Layout of the first-order  $\Sigma\Delta$ -modulator***Layout of the  $\Sigma\Delta$ -modulator with input square-wave modulation*

The  $\Sigma\Delta$ -modulators with input square-wave modulation composing the signal analyzer prototype have been laid out following the recommended guidelines for switched-capacitor circuits. Analog sub-blocks and analog signal paths are conveniently shielded from the digital circuitry. Figure 5.7 shows a diagram of the layout of one of the  $\Sigma\Delta$ -modulators. It occupies an area of  $130\mu\text{m} \times 250\mu\text{m}$ .

*B. Digital Part*

The digital part of the analyzer has not been integrated. Nevertheless, an area overhead estimation can be given. A non-optimized direct synthesis from a Verilog description of the DSP is shown in Figure 5.8. It includes the digital processing circuitry needed for both the parameter extraction from the digital signatures, and 16-bit counters (able to cope with up to  $2^{16} = 65536$  samples of the signal). A digital standard-cell library in the same  $0.35\mu\text{m}$  CMOS technology was used. It takes an area of  $300\mu\text{m} \times 300\mu\text{m}$  approximately.

FIGURE 5.8. Synthesized digital circuitry using standard-cells in a 0.35 $\mu\text{m}$  technology



### 5.2.3. Post-layout simulations

The functionality of the designed analyzer has been verified by electrical simulation of its extracted view. To provide an example of this validation, a test signal composed by three harmonic components and a DC level has been fed to the analyzer under the test conditions shown in Table 5.5. The obtained magnitude measurements are listed in Table 5.6, and are in agreement with the expected ones. The number of evaluation period has been set to 8 in these simulation to keep the simulation time low.

TABLE 5.5. Simulation conditions

Parameter	Value
Oversampling ratio, $N$	144
Full scale, $FS$	0.7V
Main component frequency, $f$	8kHz
Main component amplitude, $A_1$	500mV
Second harmonic amplitude, $A_2$	80mV
Third harmonic amplitude, $A_2$	10mV
DC level	100mV

TABLE 5.6. Simulation results

Signal component	Evaluation periods	Expected magnitude signatures	Measured signature: $\sqrt{I_{1k}^2 + I_{2k}^2}$
DC level	8	[160, 168]	166
$A_1$	8	[520, 528]	523
$A_2$	8	[80, 88]	86
$A_3$	8	[6, 14]	9

### 5.3. Prototype characterization

The described signal analyzer was integrated in the selected  $0.35\mu\text{m}$  CMOS technology. Figure 5.9 shows a microphotograph of the integrated demonstrator and a detail of one of the  $\Sigma\Delta$ -modulators. The system occupies an area of only  $0.065\text{mm}^2$ , excluding pads.

The general test set-up for the experimental validation of the prototype is illustrated in Figure 5.10. It makes use of the Agilent 93000 test system. This test system generates the synchronized input stimuli, digital control signals, and the master clock, provides the supply and analog reference voltages, and acquires and processes the bit-streams from the modulator outputs emulating the DSP block via software.

FIGURE 5.9. Integrated circuit microphotographs. a) General view. b) Sigma-delta modulator detail

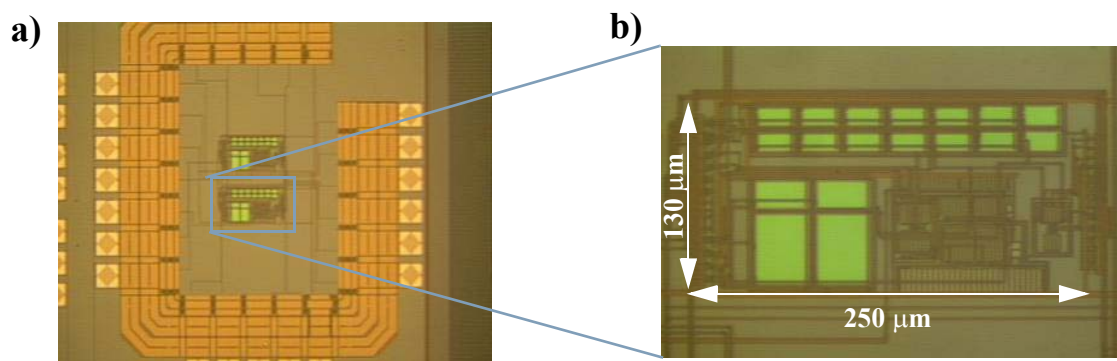
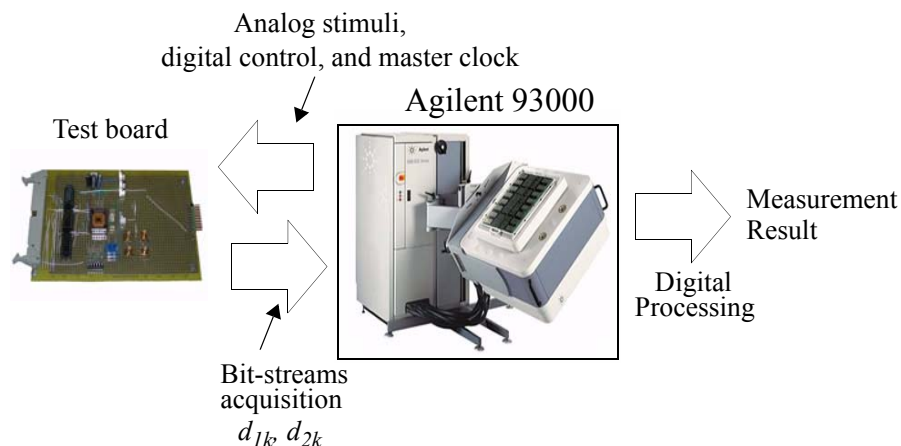


FIGURE 5.10. General test set up



Different experiments have been carried out in order to verify that the behavior of the analyzer is as theoretically described before. All the experiments have been performed under the following conditions in the analyzer: the analog ground has been set to 1.65V, which is the midpoint of the 3.3V of power supply, and the analog reference voltages in the feedback D/A converters have been set to  $V_{ref+}=2V$ , and  $V_{ref-}=1.3V$ .

The first set of experiments is designed to verify the linear behavior of the signatures with the number of samples. After that, the measurement capabilities of the system are checked by performing amplitude, phase-shift, DC-level and harmonic component measurements over a set of calibrated test signals. Finally, the repeatability of the measurements is tested by performing multiple magnitude measurements over a test signal.

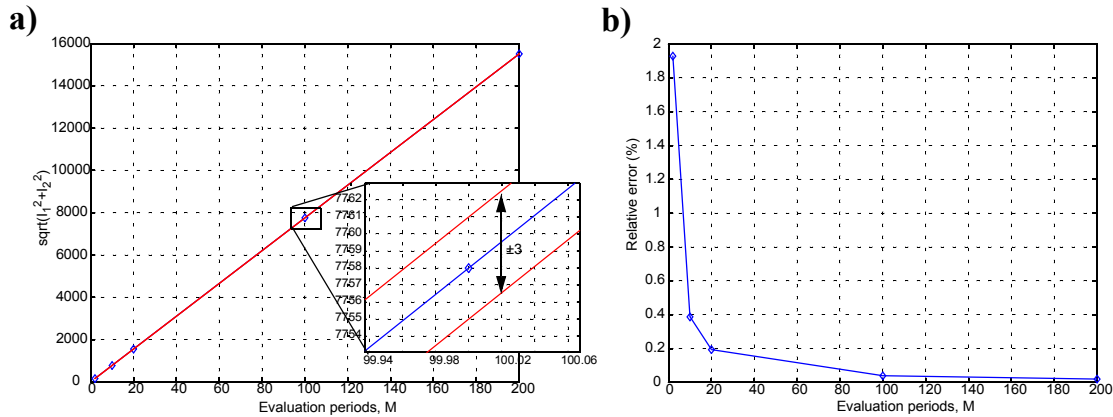
### 5.3.1. Dependency with the number of evaluation samples

From (4.34), given that the unknown error terms,  $\varepsilon_{1k}, \varepsilon_{2k}$ , are limited to  $\varepsilon_{1k}, \varepsilon_{2k} \in [-4, 4]$ , it can be derived that the magnitude signature defined as  $\sqrt{I_{1k}^2 + I_{1k}^2}$  verifies,

$$\sqrt{I_{1k}^2 + I_{1k}^2} \in \left[ \frac{MN2A_k}{\pi} - 4, \frac{MN2A_k}{\pi} + 4 \right] \tag{5.6}$$

where it has been assumed that  $A_i \gg A_j$  for each  $i < j$ . A linear behavior of the magnitude signature with the number of evaluation samples,  $MN$ , is then expected under these conditions. To check this behavior a single tone of around 600mV was fed to the analyzer block, and different magnitude

FIGURE 5.11. a) Obtained amplitude digital codes vs. number of evaluation periods.  
b) Relative error of the measurements



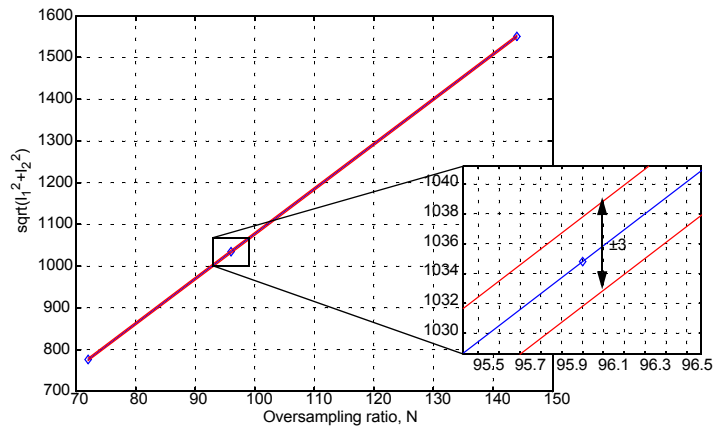
measurements were performed sweeping the number of evaluation periods,  $M$ , and the oversampling ratio in the modulators,  $N$ .

Figure 5.11a represents the obtained digital codes corresponding to the amplitude measurement for different number of periods taken for the evaluation. The sampling frequency is set to 1MHz, and the oversampling ratio to  $N=144$ . As expected, all the codes are confined in a band that have a linear characteristic with error bounds limited to  $\pm 3$ , what is in agreement with the maximum expected error of  $\pm 4$ . Figure 5.11b shows the evolution in this case of the relative error versus the number of evaluation periods, where it can be seen how this relative error decreases drastically, as expected, with the number of samples. Table 5.7 summarizes the measurements in Figure 5.11 together with the expected intervals for each measurement calculated according to (4.34). The agreement between the expected and obtained measurements is very good.

TABLE 5.7. Amplitude measurements as a function of the number of evaluation periods

$M$	$\sqrt{I_1^2 + I_2^2}$	Expected window
2	155	[151, 159]
10	775	[772, 780]
20	1550	[1548, 1556]
100	7758	[7755, 7763]
200	15518	[15514, 15522]

FIGURE 5.12. Obtained amplitude digital codes vs. oversampling ratio



Similarly, Figure 5.12 shows the obtained digital codes corresponding to the amplitude measurement for the same input stimulus, but for different oversampling ratios. The number of evaluation periods is fixed to  $M=20$ . Again, all the codes are confined in a  $\pm 3$  error band, as expected according to the theoretical analysis. Table 5.8 lists the measurements in Figure 5.12 together with the expected intervals from (4.34). Again, there is a good agreement between measurements and theory.

TABLE 5.8. Amplitude measurements as a function of the oversampling ratio

N	sqrt(I <sub>1</sub> <sup>2</sup> +I <sub>2</sub> <sup>2</sup> )	Expected window
72	777	[772, 780]
96	1035	[1031, 1039]
144	1550	[1548, 1556]

### 5.3.2. Amplitude, phase-shift, and DC-level measurements

A single tone whose amplitude was swept from around 2mV to 600mV was fed to the prototype. Figure 5.13a shows the obtained digital codes corresponding to the different measurements of amplitude. The number of samples is fixed to  $N=144$  and  $M=20$ . Again the linear characteristic of the codes and error bands limited to  $\pm 3$  agrees with the discussed theoretical performance. Figure 5.13b shows the relative error of this measurement as a function of the input amplitude. As expected, it decreases drastically with the amplitude of the signal.

Figure 5.14 demonstrates the phase measurement capabilities of the evaluator. The input signal in this case is a single tone of amplitude 400mV, whose phase-shift which respect to the modulating square-wave  $SQ_k^T(t)$  has been varied from around  $-10^\circ$  to  $-100^\circ$ . Figure 5.14 shows the obtained digital codes  $I_2/I_1$  versus the actual tangent of the phase shift between both signals. The number of samples is fixed to  $N=96$  and  $M=200$ . The linear characteristic of the codes and error bands limited to  $\pm 2$  agrees with the expected theoretical behavior.

The DC measurement capabilities are shown in Figure 5.15. The input of the evaluator has been set to a single-tone sinewave of amplitude 200mV and zero offset. Figure 5.15 shows a histogram of the DC-level measurements of the input signal when the number of samples is fixed to  $N=144$  and  $M=2$ . The obtained digital codes are inside the expected window in a good agreement with the theoretically expected behavior.

**FIGURE 5.13. a) Experimental results for different values of the input stimulus amplitude. b) Relative error of the measurements**

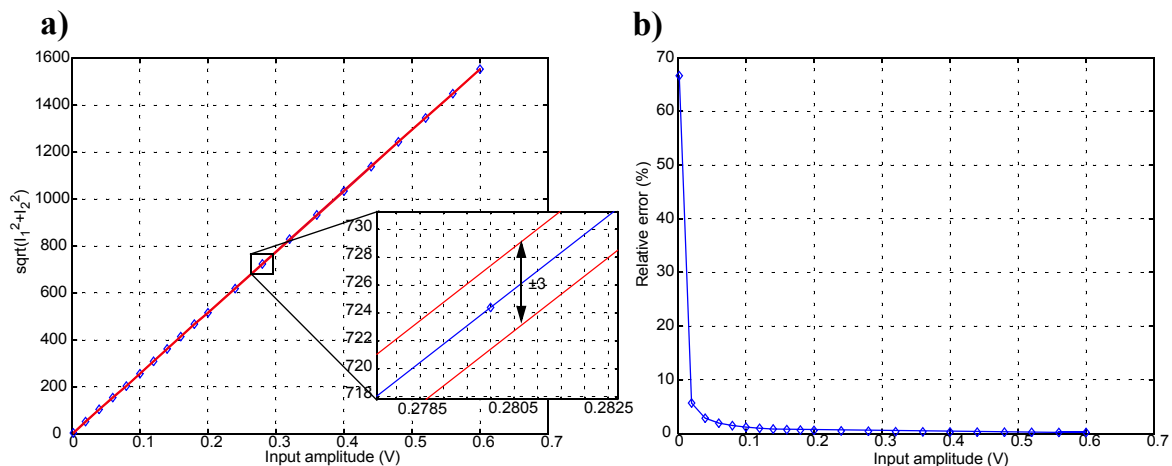




FIGURE 5.14. Experimental results for different input stimulus phase shift

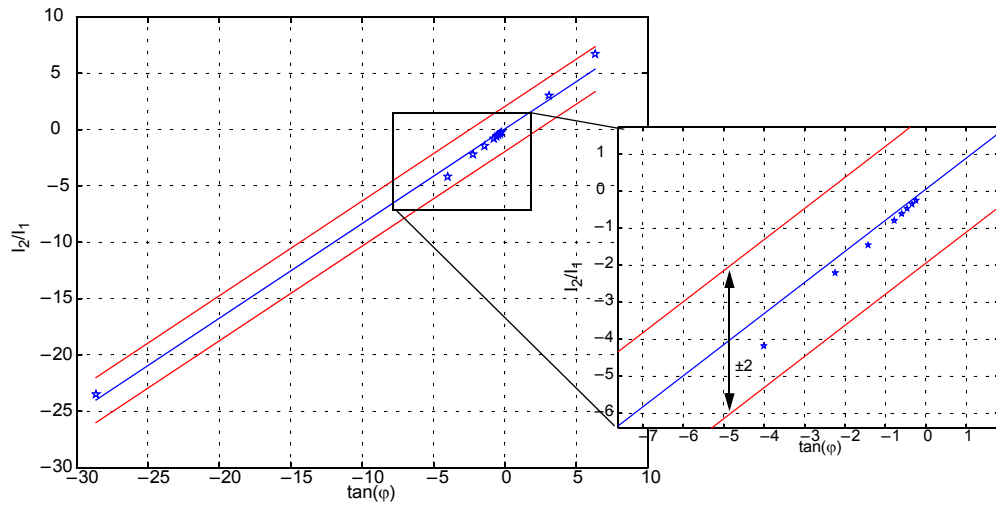
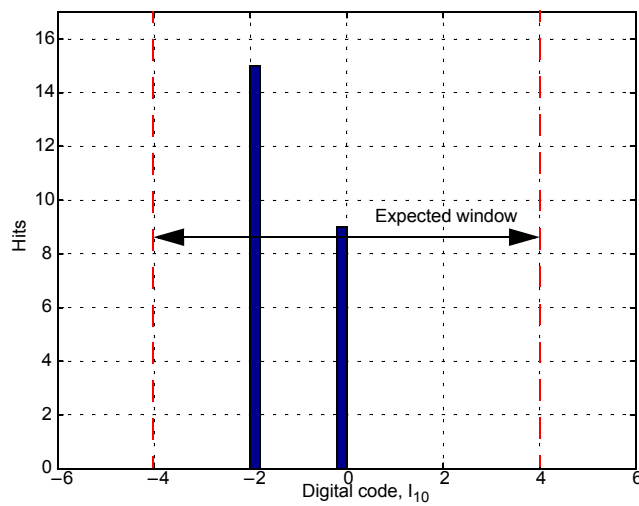


FIGURE 5.15. DC-level measurement histogram



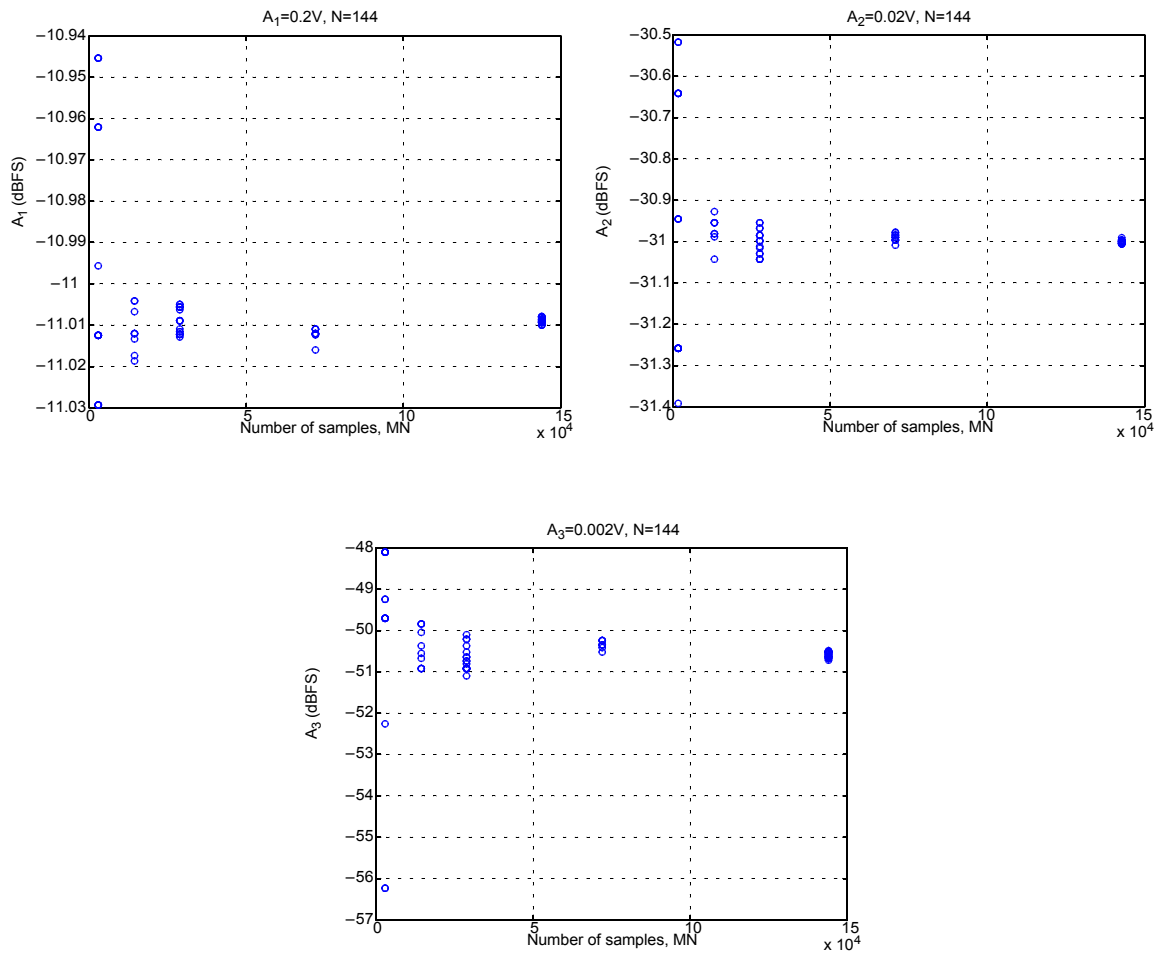
### 5.3.3. Harmonic component measurements

A multitone signal composed by three harmonic components of magnitudes  $A_1=200\text{mV}$ ,  $A_2=20\text{mV}$ , and  $A_3=2\text{mV}$  was fed to the prototype. Figure 5.16 and Figure 5.17 show the measurements relative to the full-scale of the modulator of the magnitude of each harmonic component. The oversampling ratio is fixed to  $N=144$  for Figure 5.16 and  $N=96$  for Figure 5.17 while the number of periods taken for the evaluation has been varied from  $M=20$  to  $M=1000$ . Twenty-five runs of this experiment were carried out in order to demonstrate that the measurements are repeatable. It is clear to see how the measurements of the second and third harmonic components are 20dB and 40dB below the main one, respectively. Figure 5.16 and Figure 5.17 also demonstrate how the relative error of the measurements decreases as the number of evaluation periods increases, achieving sensitivities of fractions of dBFS very quickly.

### 5.3.4. Repeatability tests

To show that the measurements are repeatable, Figure 5.18 presents three histograms for the measurements of three single tones with amplitudes 600mV, 200mV, and 20mV. The sampling frequency is set to 1MHz and the number of samples is fixed to  $N=144$  and  $M=20$ . All the obtained measurements lie inside the expected intervals in agreement with the theory.

FIGURE 5.16. Harmonic component measurements as a function of the number of samples: oversampling ratio  $N=144$



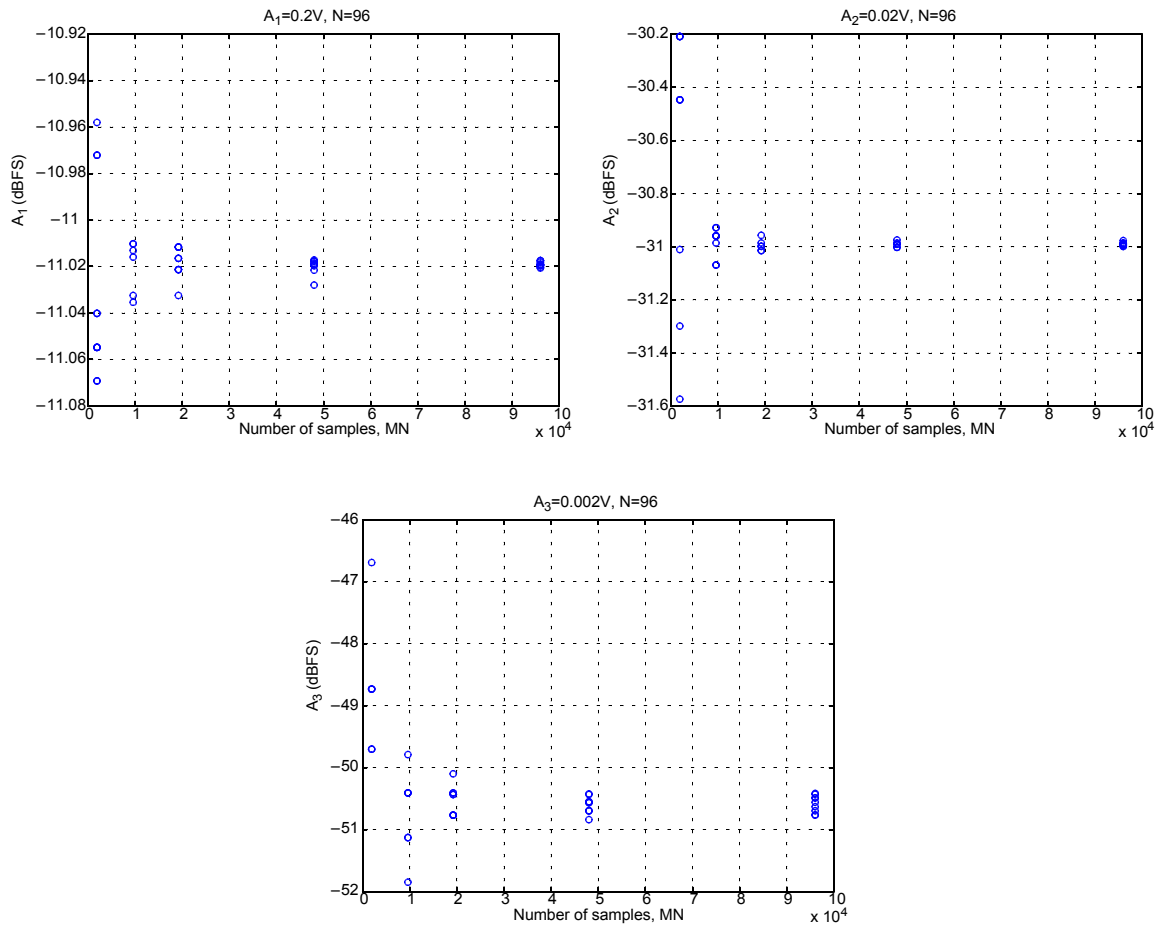
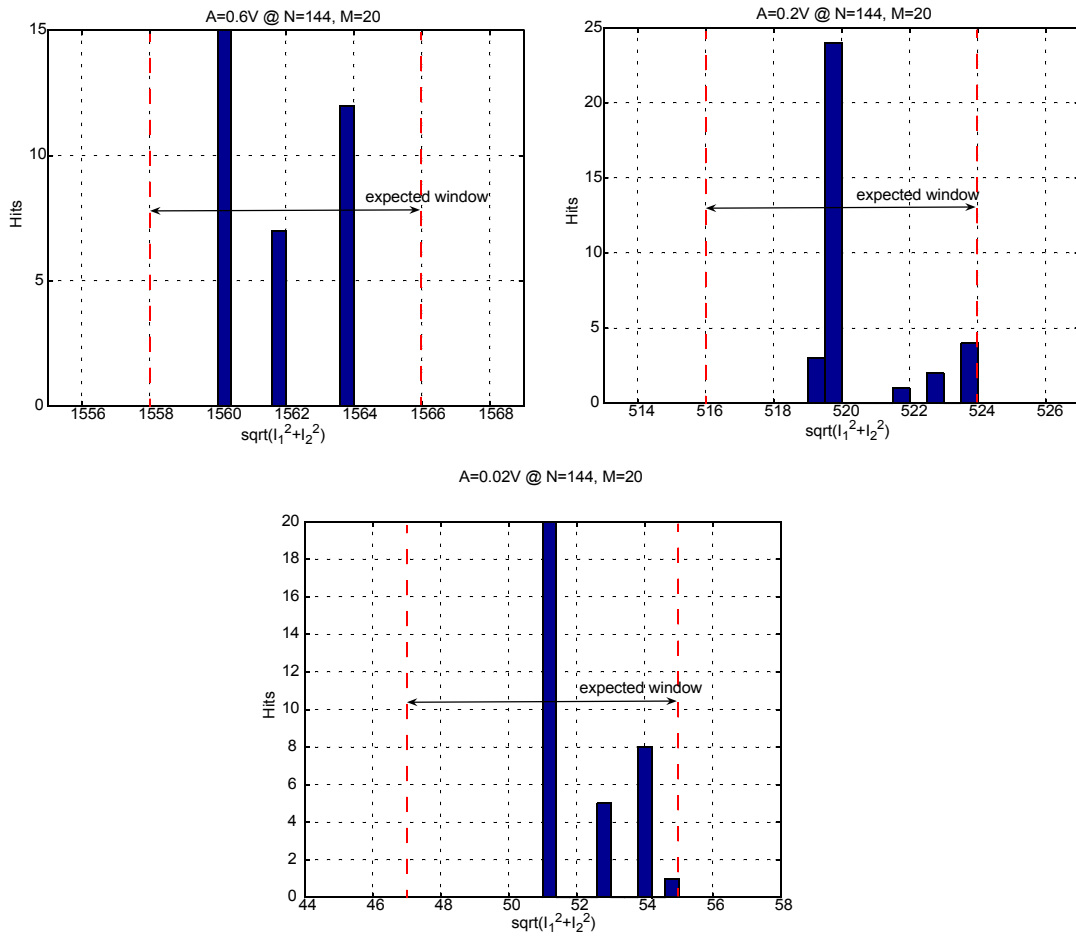
**FIGURE 5.17. Harmonic component measurements as a function of the number of samples: oversampling ratio  $N=96$** 

FIGURE 5.18. Amplitude measurement histograms



## 5.4. Summary

A prototype of the proposed periodic signal characterization scheme has been presented, together with some practical design guidelines for its efficient implementation. The developed prototype has been integrated in a standard 0.35 $\mu$ m technology.

Measurements in the lab verifies the measurement capabilities of the prototype. The integrated system is able to characterize periodic waveforms by extracting, in the digital domain, the DC level and the amplitude and phase shift of the harmonics that compose the signal. Experimental results demonstrate the viability of the approach and the agreement with the expected results. In particular, it is worth to remark the ease of controlling the accuracy of the measurements just by increasing the number of evaluated samples. In this line, sensitivities of fractions of dBFS have been demonstrated. The prototype can work at frequencies of up to 1MSample/s, what makes it suitable for the characterization of signals in the range of audio.

The developed prototype shows also the simplicity, robustness, and area efficiency of the proposed approach, what make it very suitable for BIST applications.

## A Network/Spectrum Analyzer for BIST Applications

*This chapter presents a robust digitally controlled BIST solution for the frequency characterization of analog circuits. The proposed system is based on the previously presented signal generator and analyzer. It allows a complete frequency characterization of an analog system in terms of magnitude and phase, including also harmonic distortion and offset measurements. An on-board prototype has been developed, and measurements in the laboratory support its stated functionality.*

## 6.1. Introduction

The test of most of the analog and mixed-signal subsystems composing complex SoCs usually demands the measurement of a number of frequency-related specifications such as gain, phase-shift, harmonic distortion, offset, dynamic range, etc. Because of that, the frequency response analysis and its adaptation to a full BIST scheme have become a hot research topic in the test community for the last years.

Traditional functional test methods for the frequency characterization of analog systems are based on the application of calibrated stimuli (usually sinewave signals) to the circuit under test, and the acquisition and processing of the output responses to obtain the target parameters. In this chapter, we propose a solution for the frequency characterization of analog systems based on the previously presented sinewave generator (Chapters 2 and 3) and signal analyzer (Chapters 4 and 5). As it will be demonstrated in this chapter, the combination of these test blocks results in a robust test system that can cope with a complete frequency response characterization in terms of magnitude and phase-shift, including also harmonic distortion and offset measurements. An on-board prototype of the proposed test solution is presented to show the feasibility and functionality of the approach in a practical application example.

This chapter is organized as follows: firstly, Section 6.2 presents some usual frequency characterization equipment and reviews different proposals reported in the literature for its adaptation to a BIST scheme. Section 6.3 describes the proposed test core. After that, Section 6.4 details an on-board prototype of the proposed test system, while Section 6.5 gives some experimental results. Finally, Section 6.6 summarizes the main points of the chapter.

## 6.2. Review of previous frequency characterization solutions

Functional frequency characterization solutions for BIST applications have the objective of integrating the frequency characterization test equipment on-chip. This test equipment includes, basically, spectrum analyzers and network analyzers, that are typical test equipment widely used for the frequency characterization.

Many interesting works have tried to replicate the functionality of spectrum/network analyzers within a BIST scheme, in such a way that they include a signal generator to provide the test stimulus, a signal analyzer for evaluation of the test response, and some control circuitry. In this line, several BIST techniques for frequency characterization of analog circuits have been recently reported.



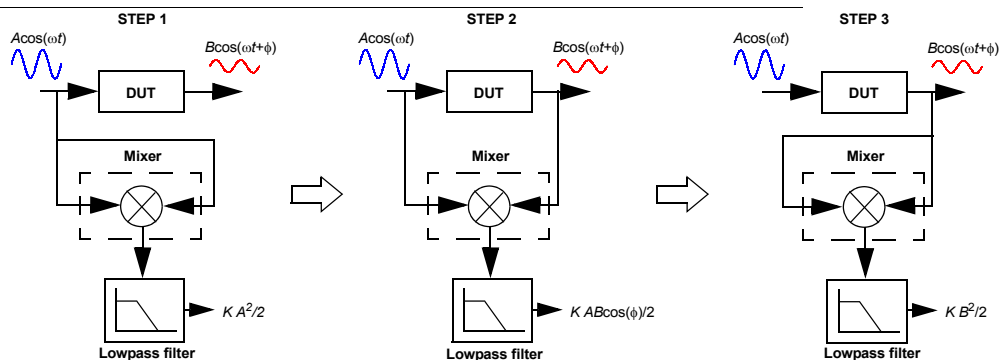
There are many different approaches. Thus, the work in [78] proposes a fully digital solution for the frequency characterization of analog circuits. It uses a direct digital synthesizer (DDS) based on a look-up table to supply test sinewaves with different frequencies and phases, while the analog output response is analyzed in the digital domain using a DSP. Although this all-digital approach offers the advantages of simplicity, robustness and reusability, it is limited by the performance and extra overhead of the unavoidable D/A and A/D converters that have to be added as interface with the analog DUT.

The work in [50] presents another approach also based on the use of digital circuitry for signal generation and evaluation. The generation of the test signal is based on the filtering of a  $\Sigma\Delta$  encoded bit-stream, and the evaluation is based on the extraction of digital signatures using a  $\Sigma\Delta$ -modulator and a set of counters. However, this work performs a signature-based on-chip evaluation of the DUT frequency response, but no functional specifications are addressed.

The proposals in [52], [70], [76], [99] try to replicate the functionality of analog spectrum/network analyzers. Thus, in [52] signal generation is based on an SC variable gain amplifier, while the amplitude of the harmonic components is extracted from the response using a programmable bandpass filter and an amplitude detector. This solution, although simple and compact, is limited to applications demanding low frequency and low dynamic range. The work in [70] also relies on a high-selectivity programmable bandpass filter, but followed in this case by an A/D converter to evaluate the test responses with an external DSP, while the signal generation is based on an analog SC oscillator. Dynamic range and frequency range are improved with respect [52], but the complexity and area overhead of the employed circuitry is also increased. The work in [76] discusses the implementation of a modulation-based spectrum analyzer for BIST applications.

High frequency applications are pursued by the network analyzer presented in [99]. Test stimuli are generated by a frequency synthesizer, while the evaluation strategy, schematically shown in Figure 6.1, is based on sequentially mixing the output and input signals of the DUT to obtain its gain

**FIGURE 6.1. Parameter extractor based on analog mixers**



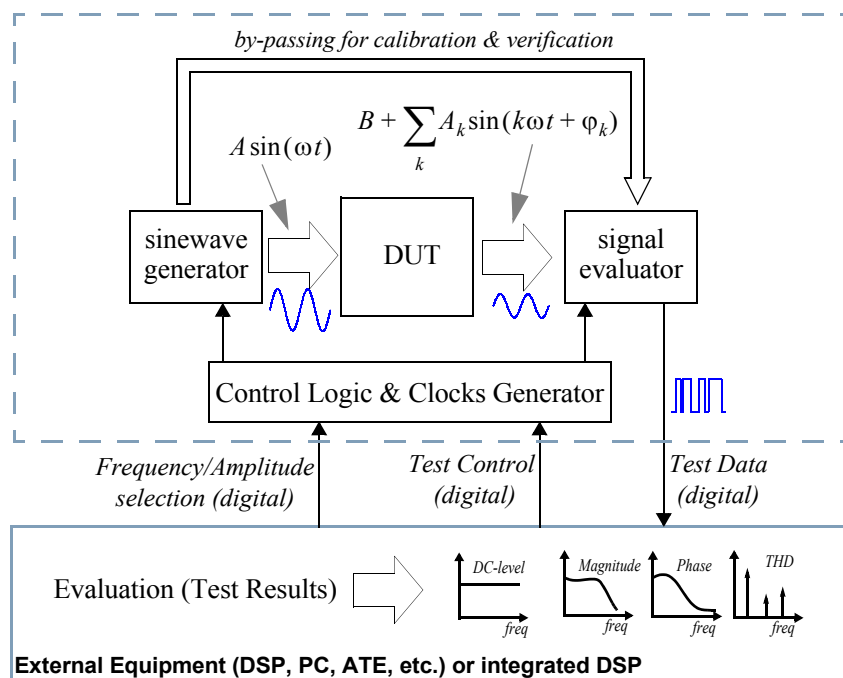
and phase shift. Although the frequency range is greatly improved (it is demonstrated in the range of hundreds MHz), this approach is limited by the dynamic range that can be achieved, and harmonic distortion measurements are not contemplated.

### 6.3. System description

Figure 6.2 shows the block diagram of the proposed test core for frequency response characterization. Apart from the DUT, it is composed by three main blocks:

- The sine wave generator with amplitude and frequency digital control presented in Chapter 2. As it was previously discussed, it is based on a filter modified to perform two operations at the same time: signal generation and filtering of unwanted components.
- The signal evaluator based on 1st-order  $\Sigma\Delta$ -modulator and digital counters presented in Chapter 4. It provides two digital words that serve as signatures from what the response parameters can be

**FIGURE 6.2. Conceptual block diagram of the proposed characterization system**



extracted by a simple digital processing. The processing of the signatures can be performed either internally, if a simple DSP is included, or externally.

- Some digital logic for control, clocks generation, and synchronism tasks as the main interface with the external test equipment.

The calibration path in Figure 6.2 has a double function: it makes possible the verification of the BIST circuitry by passing directly the generated test signal to the signal evaluator, and it also allows the calibration of the test stimulus. This calibration is essential in the functionality of a network analyzer, that has to relate the input and output of the DUT to measure performance parameters such as gain and phase-shift.

The functionality of the system can be described as follows. Firstly, the selected test stimulus generated by the sinewave generator is bypassed to the signal analyzer for self-test and calibration purposes. Then, the control logic programs the signal generator to deliver the corresponding test stimulus to the DUT. The response signal is then analyzed by the signature extractor, which generates two digital words encoding the characteristic parameters of the output signal. The obtained signatures are finally processed and related to the reference values previously acquired in the calibration stage to extract the target parameter. The combination of the developed test schemes for signal generation and evaluation gives very flexible measurement capabilities to the proposed test core. Thus, measurements of gain, phase-shift or delay, offset, and harmonic distortion are possible. These measurement capabilities will be detailed later in this chapter with a practical demonstrator prototype.

## 6.4. Prototype construction

An on-board prototype of the test system depicted in Figure 6.2 was developed to show the feasibility of the proposed approach. The on-board demonstrator makes use of the previously integrated SC discrete-time sinewave generator prototype (see Chapter 3), as the sinewave generation block, and the integrated signal analyzer prototype (see Chapter 5), as the signal evaluator block. An active-RC second-order lowpass filter has been selected as the device under test to demonstrate the measurement capabilities of the proposed test core.

In the following subsections, some general guidelines about the implementation of the test board are given, and the demonstrator board is presented.

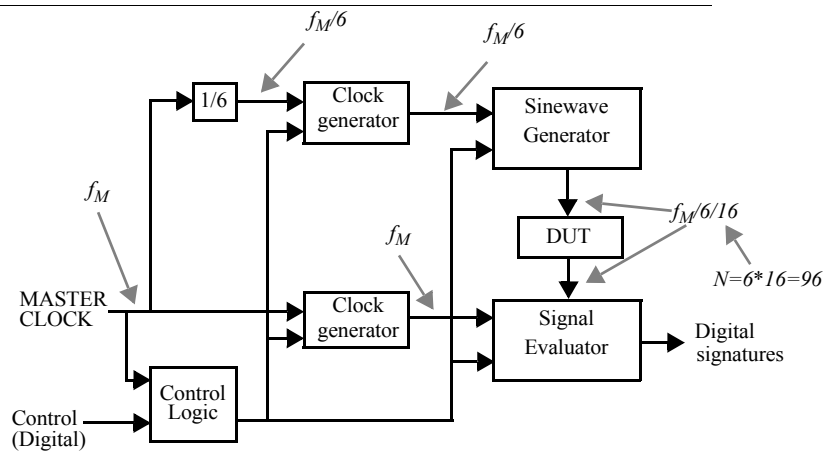
### 6.4.1. Implementation considerations

Among the building blocks composing the test core, the discrete-time signal generation block and the signal evaluation block were extensively detailed in previous chapters. The operation ranges of the included generator and evaluator blocks make the prototype able to characterize analog circuits in the frequency range of audio. It is also worth to mention that a reconstruction filter has not been included after the SC discrete-time sinewave generator. The test signals are then composed by the desired frequency component and the corresponding spectral replicas due to the sampling. However, it can be easily proved that the spectral replicas have little or no impact at all in the computation of the signatures (see Appendix 4). The only building block in the prototype that demand additional attention is the control logic and clock generator.

The control logic and clock generator block, apart from generating the necessary control signals for both the generation and evaluation cores, has the mission of assuring the indispensable synchronization between the signal generator and the signature extractor. Let us remember that the developed signal characterization strategy demands coherence and synchronization between the signal to be evaluated and the sampling clock in the modulators that compose the signature extractor. Only if this coherence and synchronization are assured, it is then possible to use equations (4.33)-(4.35) to characterize the test signals.

A block diagram of the control and synchronization logic is illustrated in Figure 6.3. An important advantage of the proposed characterization system is that the required coherence and synchronization is achieved by construction when the same master clock is used to generate the clocks and control signals for the signal generator and the signature extractor blocks. Thus, a master clock at frequency  $f_M$  is used directly to generate the clocks and control signals for the signal analyzer, while a  $1/6$  division of the master clock is used in the generation of the clocks and control signals for the generator. Since the signal generator provides a signal of frequency  $1/16$  of its clock

FIGURE 6.3. Example of synchronization between signal generation and evaluation



frequency, that is,  $f_M/6/16$ , the oversampling ratio in the modulators is accurately set to  $N = 6 \times 16 = 96$ .

#### 6.4.2. Demonstrator board

Figure 6.4 shows a photograph of the developed demonstrator board, together with a schematic of its floorplanning. It includes the discrete-time SC generator, the integrated signal analyzer, the discussed clock generator block, and a filter as the DUT.

The selected DUT is an active-RC second-order lowpass filter, build from commercial ICs and electrical components. Figure 6.5 shows the schematic of the DUT. The selected amplifier IC is a commercial fully-differential audio operational amplifier, model OPA1632 fabricated by Texas Instruments. The resistance values  $R$  have been set to  $R=20\text{k}\Omega$ , and the capacitances  $C$  have been set to  $C=6800\text{pF}$ , which gives a cut-off frequency of around 1kHz. The performance of the developed filter will be detailed in the following section, together with the verification of the test core.

The interface with the tester is completely digital, apart from the analog supply voltages and reference voltages. Additional test points have been placed at specific nodes to allow the monitoring of selected signals, and the external injection of test stimuli.

FIGURE 6.4. On-board demonstrator

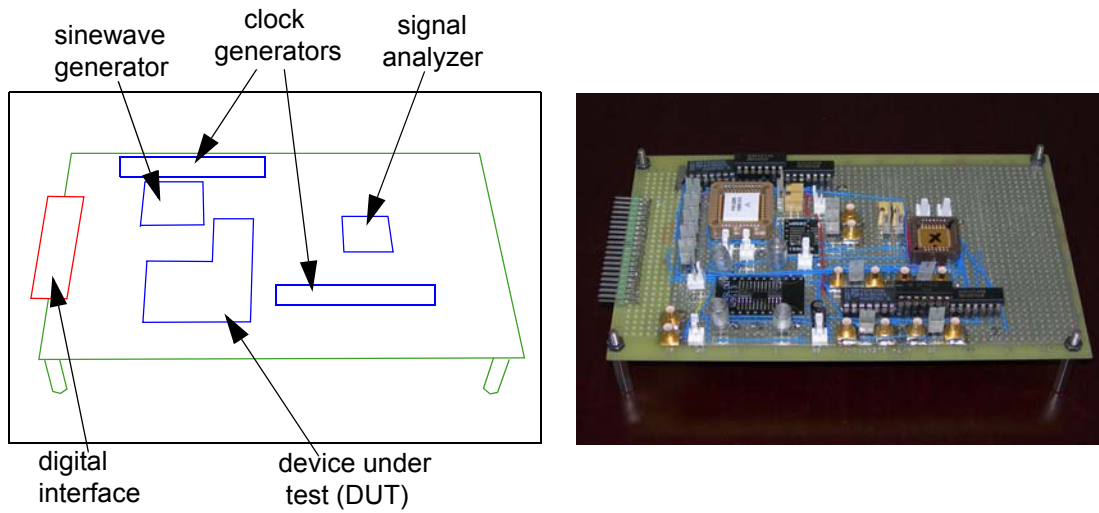
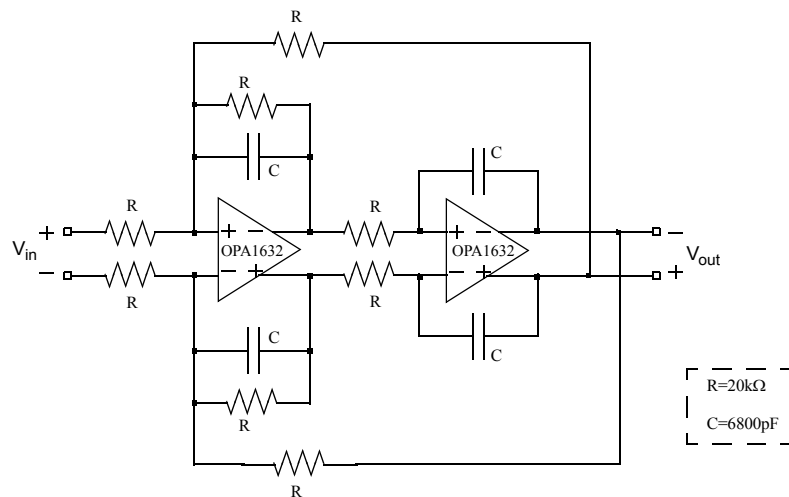


FIGURE 6.5. Block diagram of the selected DUT



## 6.5. Experimental results

This section summarizes the most significant experimental results obtained with the demonstrator board to illustrate the feasibility of the proposed test core. In the following subsections, the different measurement capabilities of the developed prototype will be detailed and supported with experimental results.

### 6.5.1. Test set-up

The general test set-up for the experimental validation of the prototype is illustrated in Figure 6.6. It makes use of the Agilent 93000 test system. This test system generates the master clock and the synchronized control signals, provides the supply voltages and analog reference voltages, and acquires and processes the bit-streams from the signal analysis block.

In order to compare the obtained measurements with some commercial equipment, the DUT was also characterized using additional test equipment. This equipment includes a LeCroy Wavesurfer 422 digital oscilloscope, and a TTI TGA-1242 arbitrary waveform generator.

### 6.5.2. Network analyzer capabilities

#### *A. Test description*

This experimental validation consisted of the measurement of the magnitude and phase Bode diagrams of the selected device under test. Firstly, a calibration of the system is performed. Due to the amplitude and phase stability of the signal generator and the inherent synchronism with respect to the control signals, this only needs to be done once. For that, the DUT is bypassed and the generated waveform fed directly to the signal evaluator. Following the protocol depicted in

**FIGURE 6.6. Test setup**

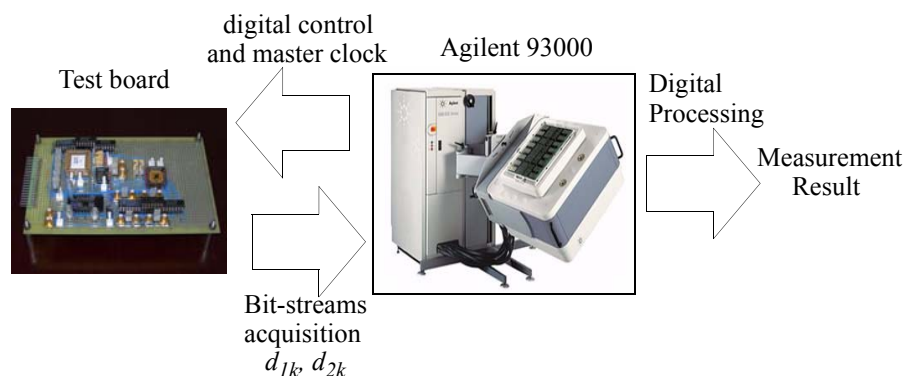


FIGURE 6.7. Test protocol for gain and phase extraction

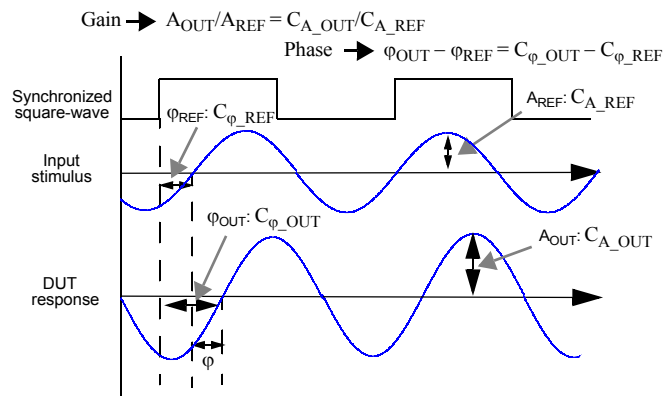


Figure 6.7, the amplitude and phase with respect the square waves used for modulation are computed and their corresponding digital codes,  $C_{A\_REF}$  and  $C_{\varphi\_REF}$ , stored to be used as references. Then, the gain of the DUT at a given frequency can be computed as the ratio of the obtained amplitude digital code,  $C_{A\_OUT}$ , and the reference code  $C_{A\_REF}$ , while the phase-shift is the difference between the obtained phase code,  $C_{\varphi\_OUT}$ , and the reference code  $C_{\varphi\_REF}$ .

In order to verify the obtained results, the magnitude and phase frequency response of the DUT was also measured using the external arbitrary waveform generator and the digital oscilloscope.

### B. Test results

Figure 6.8 shows the obtained magnitude and phase Bode diagrams obtained for different number,  $M$ , of periods used for the evaluation of each measurement. The error bands in red have been calculated accordingly to the expected windows defined by (4.34) and (4.35), while the blue stars mark each measurement. The solid line in green represent the measurement obtained with the external commercial equipment. The agreement between both measurements is very good.

Concerning the relative error in the measurements, as expected, it increases as the response magnitude decreases, and decreases as the number of evaluation periods increases. As an example of the accuracy of the proposed test core, the absolute errors in the measurements keep below 0.5dB or  $2.5^\circ$  up to 10kHz for 200 evaluation periods, and below 1.2dB or  $6.6^\circ$  in all the measured frequency range. If a better precision is needed, it can be achieved increasing the number of evaluation periods.



FIGURE 6.8. Measured Bode gain and phase diagram. Number of evaluation periods,  $M$ : a)  $M=2$ ; b)  $M=20$ ; c)  $M=40$ ; d)  $M=100$ ; e)  $M=200$

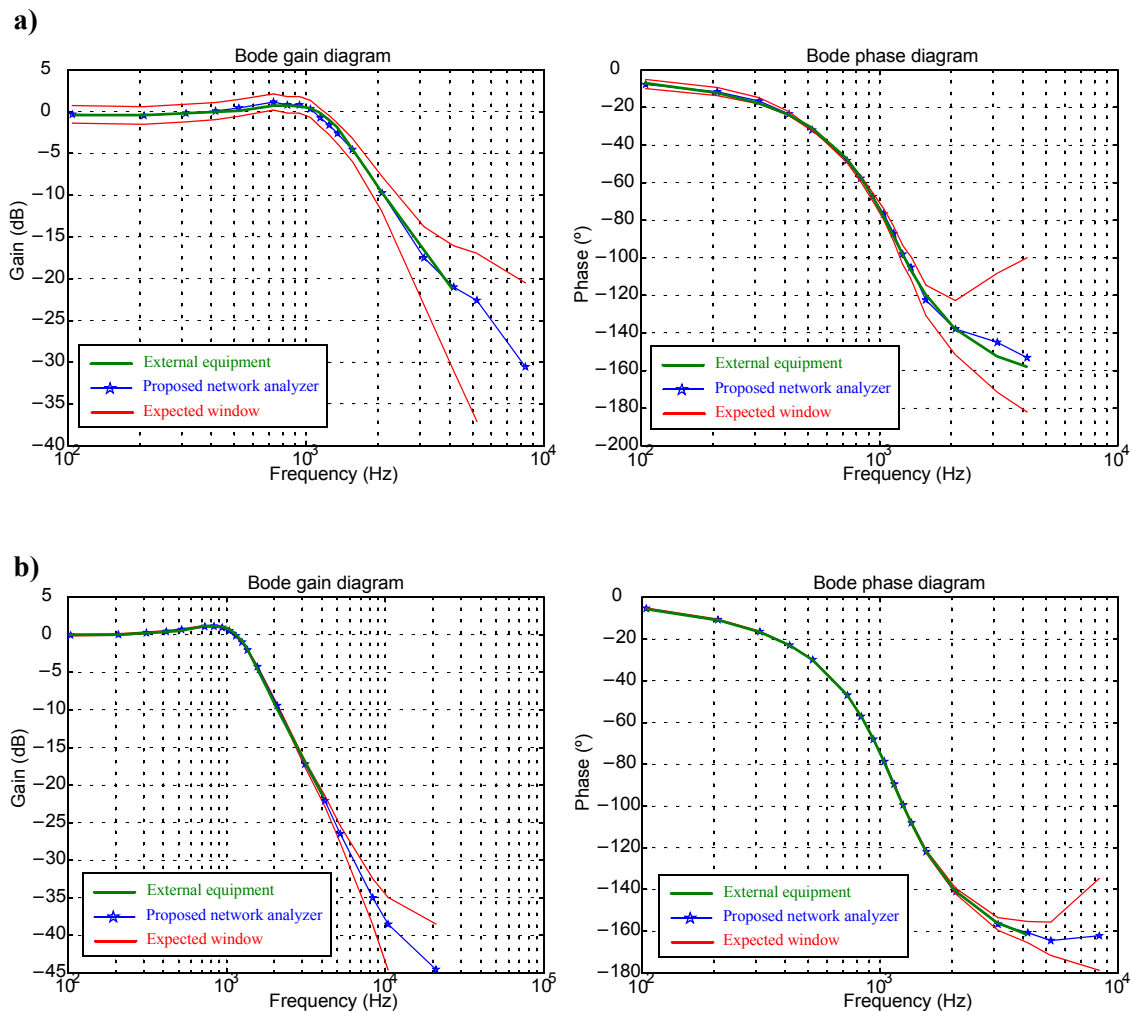


FIGURE 6.8. (cont.) Measured Bode gain and phase diagram. Number of evaluation periods,  $M$ :  
 a)  $M=2$ ; b)  $M=20$ ; c)  $M=40$ ; d)  $M=100$ ; e)  $M=200$

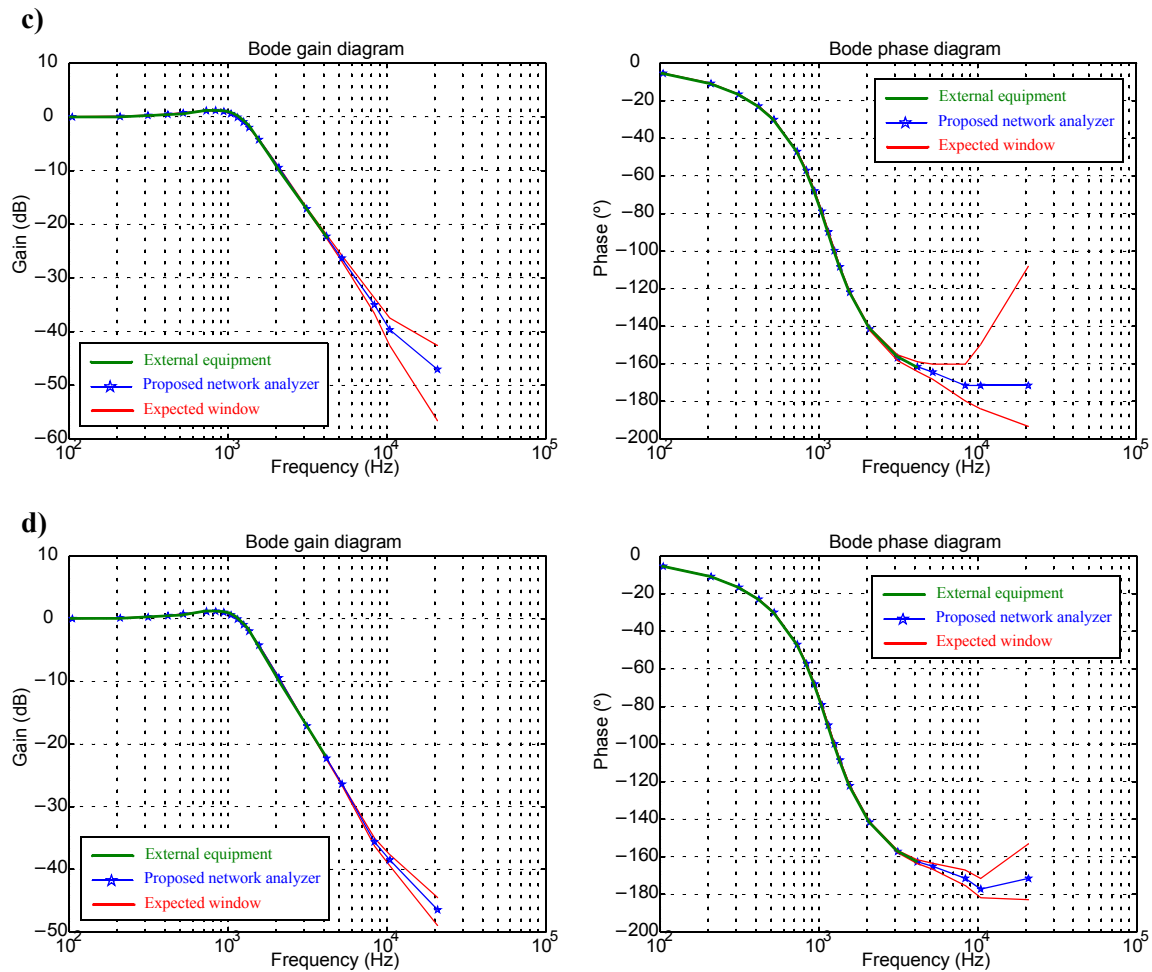
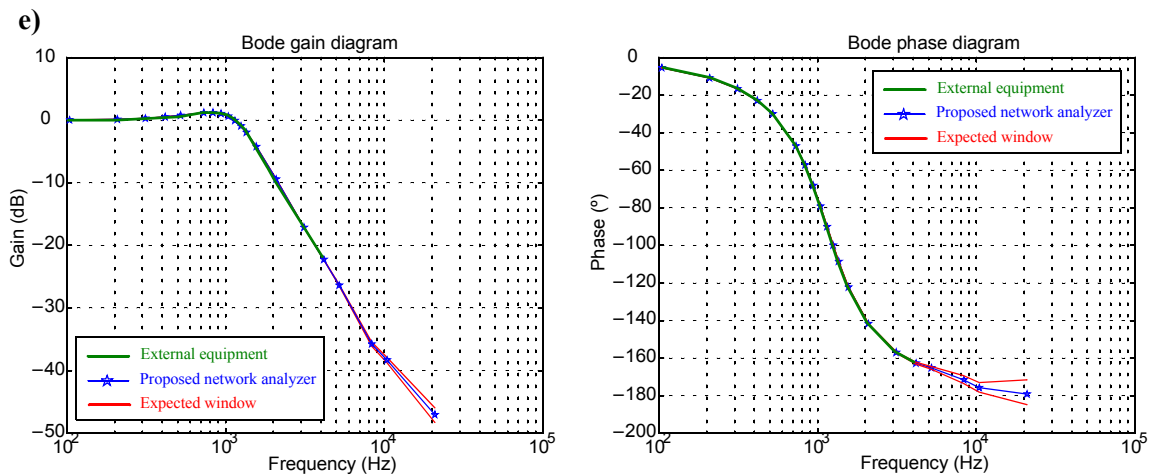


FIGURE 6.8. (cont.) Measured Bode gain and phase diagram. Number of evaluation periods,  $M$ : a)  $M=2$ ; b)  $M=20$ ; c)  $M=40$ ; d)  $M=100$ ; e)  $M=200$



### 6.5.3. Spectrum analyzer capabilities

#### A. Test description

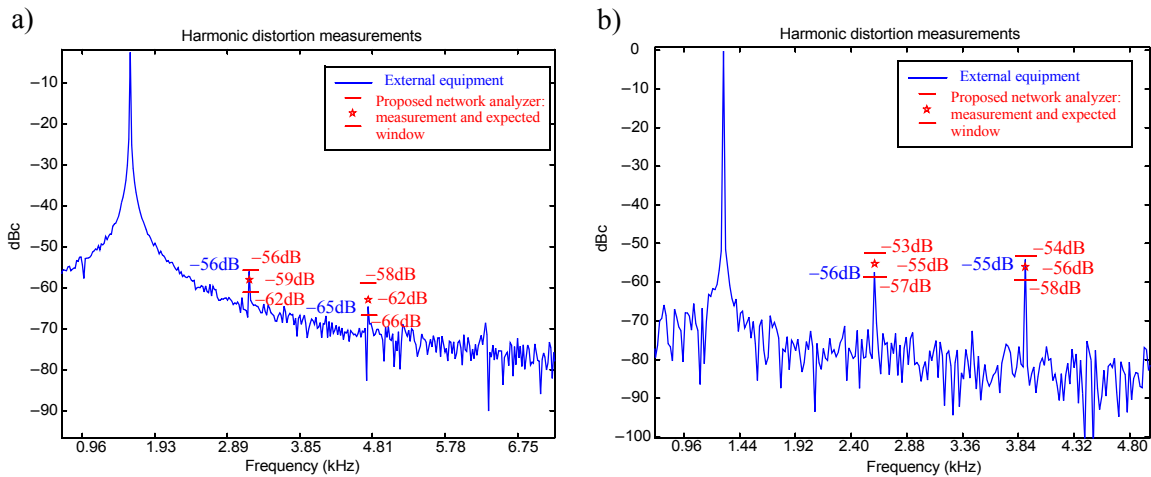
The complete system has been also validated as performing a spectrum analyzer. This experimental test consisted of the measurement of the main component, second harmonic component, and third harmonic component of the output signal of the DUT when it is excited by a sinusoidal input at different frequencies. The test stimulus is provided by the integrated sinewave generator, and the output response of the system is processed by the signal analyzer, which is configured to sequentially extract the amplitude digital codes corresponding to the magnitudes of the main component, the second harmonic, and the third harmonic. The second and third harmonic distortion are then obtained from the ratios of their corresponding digital code and the main component code.

In order to verify the obtained results, the spectrum was also measured with the external arbitrary waveform generator and digital oscilloscope.

#### B. Test results

The obtained results are illustrated in Figure 6.9. This figure shows two measurements of the second and third harmonic components of the filter output at two different frequencies, 1.6kHz and

**FIGURE 6.9. Harmonic distortion measurements: a) Main tone frequency = 1.6kHz; b) Main tone frequency = 1.3kHz**



1.3kHz, when its input is set to a 800mVpp sinewave. In both cases, the solid line is the spectrum measured with the external signal generator and the digital oscilloscope, while the stars correspond to the proposed analyzer taking 400 periods of the signal for evaluation. In the case in Figure 6.9a, the oscilloscope gives  $-56\text{dB}$  for the second harmonic and  $-65\text{dB}$  for the third one, while the proposed analyzer gives  $-59\text{dB} \pm 3\text{dB}$  and  $-62\text{dB} \pm 4\text{dB}$  respectively (error terms estimated for 400 periods). In Figure 6.9b, the oscilloscope gives  $-56\text{dB}$  for the second harmonic and  $-55\text{dB}$  for the third one, while the proposed analyzer gives  $-53\text{dB} \pm 2\text{dB}$  and  $-55\text{dB} \pm 2\text{dB}$ , respectively. The agreement between both sets of measurements is very good.

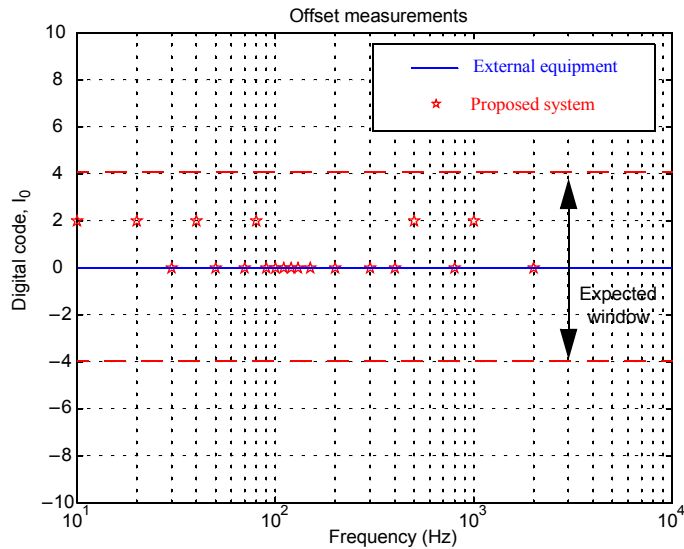
#### 6.5.4. Offset measurement capabilities

##### *A. Test description*

This test consisted of the measurement of the output offset of the DUT. The offset of the filter has been evaluated as the difference between the digital code of the DC level of the input signal, obtained in the calibration stage, and the digital code of the DC level of the output signal.

This output offset was also measured with the external generator and oscilloscope for verification purposes.

FIGURE 6.10. Filter offset measurements



*B. Test results*

Figure 6.10 shows the obtained offset measurements versus the frequency of the input signal used for the evaluation. The frequency of the input signal has been varied from a few Hertz to 20kHz, the same frequency range considered for the evaluation of the Bode diagrams. The solid line represents the offset level measured with the external generator and the digital oscilloscope, while the stars correspond to the proposed analyzer taking 2 periods of the signal for evaluation, and the red band represents the expected measurement range predicted by (4.33). The agreement between the measurements is very good.

## 6.6. Summary

A BIST solution for frequency characterization of analog circuits has been presented. The proposed system is a direct application of the previously presented signal generation and signal analysis schemes. The functionality of the proposed test core allows a complete frequency characterization in terms of magnitude and phase, including harmonic components and offset measurements.

An on-board prototype has been developed to show the feasibility of the proposed approach. This demonstrator board includes the previously integrated SC discrete-time sinewave generator, the integrated signal analysis blocks, some digital control circuitry, and a second-order filter as a demonstrator DUT.

Practical tests in the laboratory demonstrate the feasibility of the approach, and its measurement capabilities as a network analyzer, spectrum analyzer, and offset measurements. Table 6.1 provides a comparison with other reported solutions on analog built-in test systems that have been also demonstrated experimentally. Table 6.1 is aimed just to place the achieved results into perspective. Not all these approaches have the same application scenarios and capabilities, so a face-to-face comparison has no sense.

The integrated test core presented in [83] is mainly digital and very versatile what make it very attractive. However, due to the required oversampling in the generator, the applications are limited to an small fraction of the clock frequency (20MHz reported), while a large filtering is required to obtain high quality sinewaves (not included in the reported area). On the other hand, a digitizer captures analog signals with effective sampling rate of 4 GHz through subsampling, but all processing, such us FFT for frequency characterization, must be done externally.

The works in [78] and [81] present fully digital approaches for frequency characterization. Both approaches have been demonstrated with FPGA-based implementations. The use of digital circuitry gives very desirable properties to these approaches, such as robustness, design automation and reusability, however, their main limitation comes from the unavoidable A/D and D/A interfaces with the analog DUT that have to be included.

The work in [50] present also a digital approach for frequency response characterization based on SD modulation for signal generation and analysis. However, the presented test core performs only a structural test, and the measurement of functional specification is not addressed.

The test core presented in [70] present a SC analog spectrum analyzer based on an analog oscillator to provide the test stimulus, and a bandpass filter plus and A/D converter to extract the frequency response. Magnitude frequency response and harmonic distortion is contemplated, and a SFDR of 60dB at 150kHz is demonstrated with an integrated prototype.

TABLE 6.1. Comparison with other integrated analog test solutions

	Generation technique	Evaluation technique	Measurement capability	Demonstrated performance (dynamic range)	Technology and area
<b>Integrated mixed-signal test core [83]</b>	Filtered $\Sigma\Delta$ -encoded arbitrary waveform.	Response capture through subsampling	External processing required	61dB@20kHz (20MS/s)	0.35 $\mu$ m CMOS 0.67mm <sup>2</sup> (filter not included)
<b>Frequency response extractor [78]</b>	Direct digital synthesizer	Digital signal processing	Frequency response: magnitude and phase	Limited by required ADC and DAC	FPGA
<b>High resolution spectral analyzer [81]</b>	not contemplated	Goertzel algorithm	Measurement of a finite set of spectral lines	Not reported	FPGA
<b>Digital frequency testing core [50]</b>	Filtered $\Sigma\Delta$ -encoded arbitrary waveform.	$\Sigma\Delta$ signature extractor	Structural test	No functional measurement	0.18 $\mu$ m CMOS (area not reported)
<b>On-chip spectrum analyzer [70]</b>	SC analog oscillator	Programmable SC bandpass filter plus ADC	Magnitude response including harmonics	60dB@150kHz	0.35 $\mu$ m CMOS 0.9mm <sup>2</sup>
<b>Frequency response characterization system [99]</b>	Continuous-time frequency synthesizer	Mixer plus amplitude and phase detectors	Magnitude and phase of the main tone	30dB@130MHz	0.35 $\mu$ m CMOS 0.3mm <sup>2</sup>
<b>SC spectrum analyzer [52]</b>	SC variable-gain amplifier	SC bandpass filter plus amplitude detector	Magnitude response including harmonics	40dB@10kHz	0.5 $\mu$ m CMOS 0.5mm <sup>2</sup>
<b>This work</b>	Modified SC filter	$\Sigma\Delta$ modulation and simple DSP	Magnitude and phase response including harmonic and offset	70dB@62.kHz (1Ms/s)	0.35 $\mu$ m CMOS 0.33mm <sup>2</sup> (including DSP)

The SC spectrum analyzer in [52] is simple, cost-effective and contemplates harmonic measurement. However, it is limited to applications requiring low dynamic range (40dB@10kHz demonstrated)

The work in [99] presents a small area, digital interface, and a high frequency range (up to 130 MHz). It includes magnitude and phase measurements, but the dynamic range is limited to 30dB, and an ADC is required at the output.

The work in this thesis is the only one capable of a complete frequency characterization including magnitude, harmonic composition, phase-shift, and offset. The area has been estimated taking into account the generator (0.15mm<sup>2</sup>), the signature extractor (0.065mm<sup>2</sup>) and the estimation of the required DSP circuitry (0.09mm<sup>2</sup>) as shown in Figure 5.8 for parameter extraction from the digital signatures. The frequency range is limited by the SC technique and the need of oversampling in the signature extractor. In spite of that, it offers the best dynamic range when compared to other similar techniques.





## Conclusions

Moving the test equipment on-chip has been proved to be one successful proposal to simplify and reduce the cost of the test of analog and mixed-signal cores embedded in complex systems. The development of reusable test cores for their inclusion within a test scheme is a key point for enabling reusable BIST schemes for such systems. In this line, the main contribution of this thesis is the development and experimental validation of new schemes for the generation of analog test stimuli and for the characterization of analog test signals on-chip.

The proposed signal generation scheme is suitable for the generation of single-tone analog signals with a high spectral quality. It has the characteristics of very low hardware requirements and design effort. The whole generator is mainly reduced to a low-order filter whose input elements have been modified. In addition, its interface is completely digital, and the amplitude and the frequency of the generated signals can be easily programmed using only digital control signals.

On the other hand, the developed method for the characterization of analog signals is suitable for the complete characterization of a given periodic analog signal in terms of its dc-level, and the magnitude and phase of its harmonic components. It is based on an approximation of the Fourier series expansion. Its proposed implementation reduces its hardware requirements to a double modulation, square-wave and first-order sigma-delta, while the processing of the signal is performed in the digital domain by a very simple DSP block.

Both approaches have been validated not only from a theoretical point of view, but also based on experimental support. Design guidelines have been given for the successful integration of the proposed test cores, and silicon demonstrators have been implemented. Two prototypes of the signal

generator and a prototype of the signal analyzer were integrated in a standard CMOS technology to prove the feasibility of the approaches. Multiple experimental results are given in this thesis detailing the functionality of each prototype.

Finally, an on-board prototype of a complete test core featuring the integrated sinewave generator and signal analyzer has been also developed and verified in the laboratory. The proposed test core is able to completely characterize the frequency behavior of an analog DUT in terms of magnitude and phase, including also harmonic measurements and offset measurement capabilities. The obtained results give a wide experimental support to the feasibility of the proposed test system.

The simplicity of the proposed test cores, together with the robustness of the required hardware, their low design effort and area overhead, and their digital interface, make them very suitable for analog and mixed-signal BIST applications.

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## Publications

The results presented in this thesis have been partially published in the following works:

- M. J. Barragán, D. Vázquez, A. Rueda, “Guidelines for the design of a Sine-Wave Analyzer for BIST Applications”, Proc. of the Design of Circuits and Integrated Circuits, November 2004.
- D. Vázquez, A. Luque, M. J. Barragán, G. Leger, G. Huertas, A. Rueda, J. L. Huertas, “Sinewave Characterization Using Square-Wave and Sigma-Delta Modulation: Application to Mixed-Signal BIST”, Journal of Electronic Testing: Theory and Applications, vol. 21, pp.221-232, 2005.
- M. J. Barragán, D. Vázquez, G. Huertas, A. Rueda, J. L. Huertas, “Efficient and Accurate Analog Sinewave Generator for BIST Applications”, Inf. Dig. of Papers of the 11th IEEE European Test Symposium (ETS’06), May 2006.
- M. J. Barragán, D. Vázquez, A. Rueda, “A Sinewave Analyzer for Mixed-Signal BIST Applications in a 0.35 $\mu$ m Technology”, Proc. of the 9th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS’06), April 2006.
- M. J. Barragán, D. Vázquez, A. Rueda, J. L. Huertas, “On-Chip Analog Sinewave Generator with Reduced Circuitry Resources”, Proc. of the 49th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS’06), August 2006.
- M. J. Barragán, D. Vázquez, A. Rueda, “Practical Implementation of Sinewave Generators for Mixed-Signal BIST”, Proc. of the 8th Latin American Test Workshop (LATW’07), 2007.



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## Publications

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- M. J. Barragán, D. Vázquez, A. Rueda, “Practical Implementation of a Network Analyzer for Analog BIST”, Proc. of the Design Automation and Test in Europe (DATE’08), 2008.
- M. J. Barragán, D. Vázquez, A. Rueda, “Guidelines for the Design of Sinewave Generators for BIST Applications”, Proc. of the XV Iberchip Workshop (IWS’09), 2009.
- M. J. Barragán, D. Vázquez, A. Rueda, “Practical Test Cores for the On-Chip Generation and Evaluation of Analog Test Signals: Application to a Network/Spectrum Analyzer for Analog BIST”, Accepted for publication in the Proc. of the 5th IEEE International Conference on PhD Research in Microelectronics and Electronics, (PRIME’09), 2009.

## APPENDIX 1

## On-chip generation of the control signals for the proposed sinewave generation technique

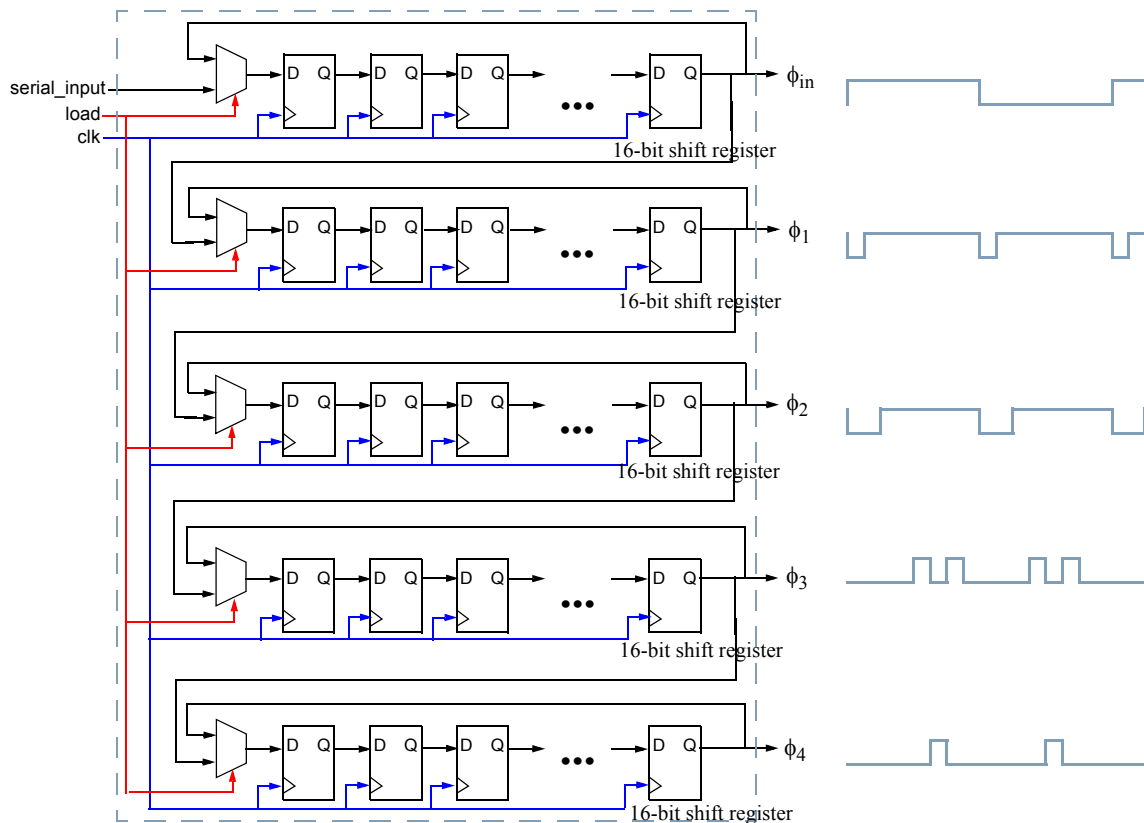
A BIST solution should contemplate the attributes of low speed digital interface needs, reduced to control and synchronization tasks. Regarding the proposed signal generation technique, it is based on programming the input elements of an analog filter. As it was discussed in Chapters 2 and 3, this can be performed in a very feasible and reliable way by applying digital words through a fully digital interface to a number of different programmable devices for the most common integrated filter design styles. This programming style produce step-wise variations of the filter input devices. Indeed, theoretical analysis concludes that very good performance can be obtained with a low number of step levels, which also means that a low number of bits are required for programming tasks. In addition, thanks to the symmetry properties of sinewave functions, these control signals are also periodical (see, for instance, the control signals of the implemented OTA-C and SC prototypes given in Figure 3.6c and Figure 3.22c, respectively) which opens the possibility of easily generating the control signals on-chip.

This appendix gives a proposal for the on-chip generation of these programming signals. Figure A1.1 shows this proposal adapted for the generation of the programming signals of the OTA-C generator prototype (a completely analogous one can be developed for the SC case), based on a simple shift register with a feedback loop, which is a simple and compact way of generating periodic bit streams. This generation technique also ensures synchronization with an external master clock, which may be a desirable characteristic in some test applications. The serial data input pin loads one period of the  $\phi_i$  signals into the shift registers sequentially when the *load* signal is high, and the stored signals are repeated periodically when the *load* signal goes down. Note that the serial input

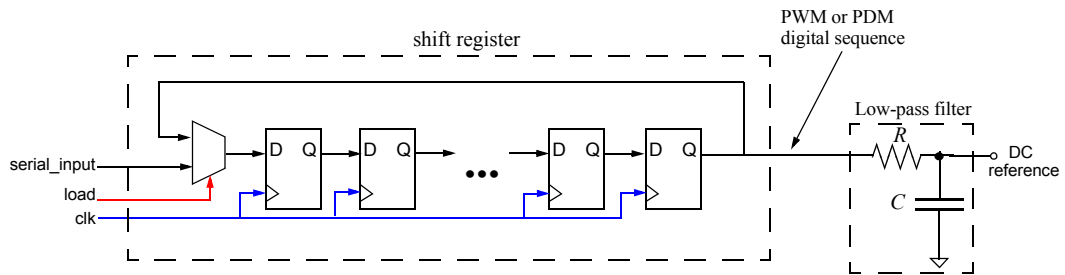
can be avoided by applying *reset* or *set* signals to the flip-flops composing each shift register. Some re-programmability is lost, but test time is reduced. Anyway, a high frequency clock may be used during the loading stage, so the loading time can be neglected for most applications.

The need of an external DC-input for amplitude control can be avoided by generating it either internally or externally through digital techniques. For instance, using the well known technique based on the integration of a digital sequence suggested in [100]. This technique represents an efficient and robust method for generating accurate on-chip DC references. It is based on filtering a digital pulse-width-modulated (PWM) or pulse-density-modulated (PDM) sequence in order to extract its average (DC) value. Figure A1.2 illustrates a possible implementation of the reference generator. It is based also on a simple shift-register and a passive RC filter, which makes possible its

**FIGURE A1.1. Example of the on-chip generation of the control signals of the OTA-C prototype**



**FIGURE A1.2. On-chip generation of the analog reference voltages through a digital interface.**



implementation together with the control signal generator previously discussed. Figure A1.2b shows a conceptual example of this approach.

Combining the generation of the digital control signals and the DC reference voltages, the interface with the external equipment can be made purely digital. Moreover, since the required hardware is mainly reduced to a set of shift registers, it may be possible in some applications to reuse existing resources to minimize the area overhead of the test circuitry. For instance, in any system compliant with the IEEE 1149.4 [21] standard for mixed-signal test bus, the boundary scan may be easily modified to generate these control signals during test mode.





## APPENDIX 2

## Differential output buffer

A differential buffer was introduced at the output of the continuous-time sinewave generator prototype. The mission of this buffer is to isolate the output nodes of the signal generator from the parasitic capacitors at the output pads, which could deviate the frequency behavior of the filter core. This appendix details the design and performance of this differential buffer.

Figure A2.1 shows the schematic of the differential buffer. It is based on a one-stage folded-cascode differential amplifier whose input stage has been replicated and properly connected to the output nodes in a feedback loop. The bias circuitry and the necessary common-mode feedback

**FIGURE A2.1. Transistor level schematic of the differential buffer**

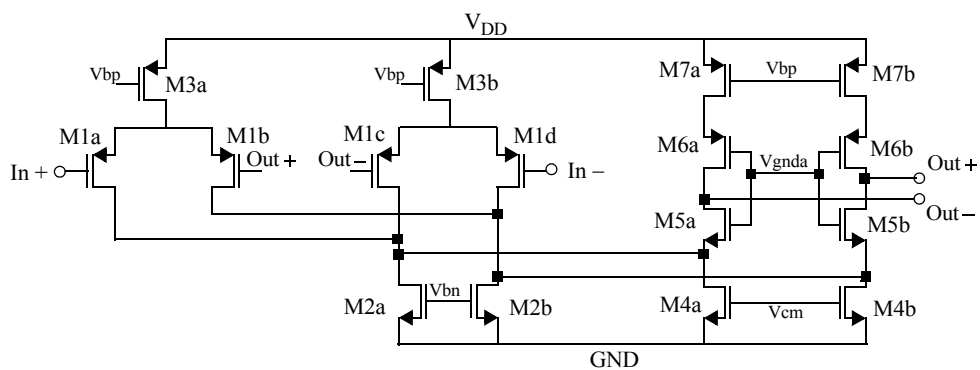
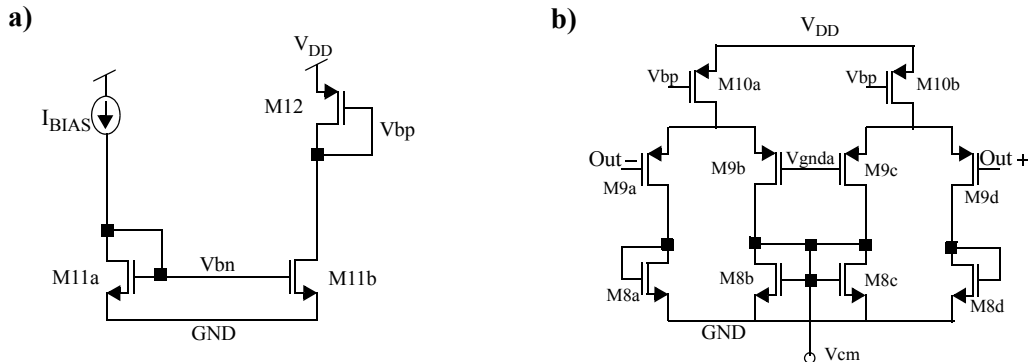


FIGURE A2.2. Transistor level schematic of the: a) bias circuitry, b) common-mode feedback circuitry



circuitry are depicted in Figure A2.2. The common mode feedback circuit senses the common mode output voltage and returns a signal through the bias line labelled  $V_{CM}$  to stabilize it to analog ground [64]. The frequency compensation is provided by the capacitance associated to the output pads, that are connected to the output nodes of the buffer. The sizes of the transistors in Figure A2.1 and Figure A2.2 are listed in Table A2.1.

TABLE A2.1. Transistor sizes for the folded-cascode stage and common mode feedback circuit

	M1	M2	M3	M4	M5	M6
$W/L$ ( $\mu\text{m}/\mu\text{m}$ )	100/0.35	64/1	200/1	64/1	64/1	200/1
	M7	M8	M9	M10	M11	M12
$W/L$ ( $\mu\text{m}/\mu\text{m}$ )	200/1	8/1	12/0.5	50/1	16/1	50/1

Table A2.2 shows the performance characteristics of the amplifier obtained by electrical simulation of the extracted view for biasing conditions  $V_{DD}=3.3\text{V}$ , and  $I_{BIAS}=200\mu\text{A}$ , and an external load of  $10\text{pF}$ .

**TABLE A2.2. Amplifier performance parameters ( $V_{DD}=3.3V$ ,  $I_{BIAS}=200\mu A$ ,  $C_{Load}=10pF$ )**

<b>-3dB-frequency</b>	300MHz
<b>Output swing</b>	2V
<b>Settling time (1%)</b>	1.6ns
<b>Slew-rate</b>	0.8V/ns
<b>THD @ 40MHz; 250mVpp</b>	70dB

The obtained performance parameters are enough to handle the output signals of the developed continuous-time sinewave generator.



## APPENDIX 3

## Computation of the test signatures

 $\hat{I}_{1k}$  and  $\hat{I}_{2k}$ 

This appendix details the calculus of the signatures  $\hat{I}_{1k}$  and  $\hat{I}_{2k}$ , that were introduced in Chapter 4 as a simplification of the Fourier coefficients computation. If  $x(t)$  is a periodic signal of period  $T$  and square-integrable over the interval  $[0, T)$ , then its signatures  $\hat{I}_{1k}$  and  $\hat{I}_{2k}$  are defined by,

$$\begin{aligned}\hat{I}_{1k} &= \frac{1}{T} \int_0^T x(t) S Q_k^T(t) dt & k = 0, 1, 2, \dots \\ \hat{I}_{2k} &= \frac{1}{T} \int_0^T x(t) S Q_k^T\left(t - \frac{T}{4k}\right) dt & k = 0, 1, 2, \dots\end{aligned}\tag{A3.1}$$

That is, signatures  $\hat{I}_{1k}$  and  $\hat{I}_{2k}$  are the continuous integration of the signal  $x(t)$  modulated by two unit-amplitude square-waves in quadrature  $S Q_k^T(t)$  and  $S Q_k^T\left(t - \frac{T}{4k}\right)$ , respectively, along a whole period of the signal  $x(t)$ . For the case  $k=0$ , it has been assumed to be  $S Q_k^T(t) = S Q_k^T\left(t - \frac{T}{4k}\right) = 1$ .

These signatures are formally similar to the Fourier coefficients, but replacing the sine and cosine eigenfunctions by a pair of square-waves in quadrature.

Signal  $x(t)$  can be expanded in its Fourier series expansion as,

$$x(t) = B + \sum_{m=1}^{\infty} A_m \sin(m\omega t + \varphi_m), \quad (\text{A3.2})$$

using the notation introduced in Chapter 4. And the square-wave  $SQ_k^T(t)$  can be also expanded in its Fourier series as,

$$SQ_k^T(t) = \frac{4}{\pi} \sum_{i=0}^{\infty} \frac{\sin((2i+1)k\omega t)}{(2i+1)} \quad k = 1, 2, \dots \quad (\text{A3.3})$$

Introducing the expansions (A3.2) and (A3.3) in the signature definitions it is simple to derive expressions for  $\hat{I}_{1k}$  and  $\hat{I}_{2k}$ . Thus, signature  $\hat{I}_{1k}$  (the computation of  $\hat{I}_{2k}$  is formally analogous) can be expressed as,

$$\hat{I}_{1k} = \frac{1}{T} \int_0^T x(t) SQ_k^T(t) dt = \frac{1}{T} \int_0^T \left( B + \sum_{m=1}^{\infty} A_m \sin(m\omega t + \varphi_m) \right) \left( \frac{4}{\pi} \sum_{i=0}^{\infty} \frac{\sin((2i+1)k\omega t)}{(2i+1)} \right) dt \quad (\text{A3.4})$$

Expanding the argument of the first summatory, it gives,

$$\begin{aligned} \hat{I}_{1k} &= \frac{1}{T} \int_0^T \left\{ B + \sum_{m=1}^{\infty} (A_m \sin(m\omega t) \cos \varphi_m + A_m \cos(m\omega t) \sin \varphi_m) \right\} \left( \frac{4}{\pi} \sum_{i=0}^{\infty} \frac{\sin((2i+1)k\omega t)}{(2i+1)} \right) dt = \\ &= \frac{1}{T} \int_0^T \left( \sum_{m=1}^{\infty} A_m \sin(m\omega t) \cos \varphi_m \right) \left( \frac{4}{\pi} \sum_{i=0}^{\infty} \frac{\sin((2i+1)k\omega t)}{(2i+1)} \right) dt \end{aligned} \quad (\text{A3.5})$$

where it has been used that sine and cosine eigenfunctions are orthogonal functions [88].

From (A3.5) it is easy to derive the signature  $\hat{I}_{1k}$  as a function of coefficients  $A_k$  and  $\varphi_k$ . Again, making use of the orthogonality, the integral can be evaluated as,

$$\hat{I}_{1k} = \frac{2}{\pi} \left( A_k \cos \varphi_k + \sum_{i=1}^{\infty} \frac{A_{(2i+1)k}}{(2i+1)} \cos \varphi_{(2i+1)k} \right) \quad k = 1, 2, \dots \quad (\text{A3.6})$$

Signature  $\hat{I}_{2k}$  can be evaluated in a similar fashion and it gives,

$$\hat{I}_{2k} = \frac{2}{\pi} \left( A_k \sin \varphi_k + \sum_{i=1}^{\infty} \frac{A_{(2i+1)k}}{(2i+1)} \sin \varphi_{(2i+1)k} \right) \quad k = 1, 2, \dots, \quad (\text{A3.7})$$

while the computation in the case  $k=0$  is trivial and it gives,

$$\hat{I}_{10} = \hat{I}_{20} = B \quad (\text{A3.8})$$





## APPENDIX 4

## On using discrete-time signals as test stimuli in the proposed spectrum/network analyzer

The developed prototype of the proposed spectrum/network analyzer makes use of a discrete-time signal generator to provide the test stimulus, without a reconstruction filter to smooth the signal. This Appendix demonstrates analytically that the use of discrete-time signals has little or no impact at all in the computation of the signatures by the signal analysis block, which justifies the choice of not including a reconstruction filter.

Let us consider a worst-case approach to the problem, in which a discrete-time sinewave of amplitude  $A_1$  and frequency  $\omega_1$  is fed directly to the signal analysis block. This discrete-time test signal will be composed by the desired frequency component at  $\omega_1$  and the corresponding spectral replicas due to the sampling at multiples of the sampling frequency. Thus, the general expression of the signatures  $I_{11}$  and  $I_{21}$ , corresponding to the main harmonic component of this signal, (similar expressions can be obtained for higher components), will be given by,

$$\begin{aligned}
 I_{11} &= \frac{2MN}{\pi} A_1 + \sum_{i=1}^{\infty} \frac{2MN}{(2i+1)\pi} C_{2i+1} \cos \varphi_{2i+1} + \varepsilon_1 \\
 I_{21} &= \sum_{i=1}^{\infty} \frac{2MN}{(2i+1)\pi} C_{2i+1} \sin \varphi_{2i+1} + \varepsilon_2
 \end{aligned} \tag{A4.1}$$

where  $M$  is the number of evaluation periods,  $N$  is the oversampling ratio in the signal analyzer,  $\varepsilon_1$  and  $\varepsilon_2$  are the quantization errors ( $|\varepsilon_x| \leq 4$ , as demonstrated in Chapter 4),  $A_1$  is the amplitude of the test sinewave (the contribution of the sampling at the fundamental frequency has been neglected),  $C_n$  is the magnitude of the frequency component of the test stimulus at frequency  $n\omega_1$ , and  $\varphi_n$  is its phase-shift. Note that, without lack of generality, it has been considered  $\varphi_1$  to be zero to simplify the calculus.

Taking into account that the test stimulus is a step-wise sinewave with  $N_L$  step levels, where  $N_L$  is a power of 2, then equation (A4.1) can be rewritten including the spectral replicas as,

$$\begin{aligned}
 I_{11} &= \frac{2MN}{\pi} A_1 + \sum_{i=1}^{\infty} \frac{2MN}{(iN_L - 1)\pi} A_1 \left| S_a\left(\frac{(iN_L - 1)\pi}{N_L}\right) \right| \cos \varphi_{iN_L - 1} + \\
 &+ \sum_{i=1}^{\infty} \frac{2MN}{(iN_L + 1)\pi} A_1 \left| S_a\left(\frac{(iN_L + 1)\pi}{N_L}\right) \right| \cos \varphi_{iN_L + 1} + \varepsilon_1 \\
 I_{21} &= \sum_{i=1}^{\infty} \frac{2MN}{(iN_L - 1)\pi} A_1 \left| S_a\left(\frac{(iN_L - 1)\pi}{N_L}\right) \right| \sin \varphi_{iN_L - 1} + \\
 &+ \sum_{i=1}^{\infty} \frac{2MN}{(iN_L + 1)\pi} A_1 \left| S_a\left(\frac{(iN_L + 1)\pi}{N_L}\right) \right| \sin \varphi_{iN_L + 1} + \varepsilon_2
 \end{aligned} \tag{A4.2}$$

where  $S_a(x)$  is the sampling function.

Equation (A4.2) can be rearranged as,

$$\begin{aligned}
 I_{11} &= \frac{2MNA_1}{\pi} \{1 + \delta_1 + \xi_1\} \\
 I_{21} &= \frac{2MNA_1}{\pi} \{\delta_2 + \xi_2\}
 \end{aligned} \tag{A4.3}$$

where the error coefficients  $\delta_1$ ,  $\delta_2$ ,  $\xi_1$ , and  $\xi_2$  are given by,

$$\begin{aligned}
\delta_1 &= \sum_{i=1}^{\infty} \frac{1}{(iN_L - 1)\pi} \left| S_a\left(\frac{(iN_L - 1)\pi}{N_L}\right) \right| \cos \varphi_{iN_L - 1} + \sum_{i=1}^{\infty} \frac{1}{(iN_L + 1)\pi} \left| S_a\left(\frac{(iN_L + 1)\pi}{N_L}\right) \right| \cos \varphi_{iN_L + 1} \\
\xi_1 &= \frac{\pi}{2MNA_1} \varepsilon_1 \\
\delta_2 &= \sum_{i=1}^{\infty} \frac{1}{(iN_L - 1)\pi} \left| S_a\left(\frac{(iN_L - 1)\pi}{N_L}\right) \right| \sin \varphi_{iN_L - 1} + \sum_{i=1}^{\infty} \frac{1}{(iN_L + 1)\pi} \left| S_a\left(\frac{(iN_L + 1)\pi}{N_L}\right) \right| \sin \varphi_{iN_L + 1} \\
\xi_2 &= \frac{\pi}{2MNA_1} \varepsilon_2
\end{aligned} \tag{A4.4}$$

Coefficients  $\delta_1$  and  $\delta_2$  represent the relative weight of the spectral replicas in the computation of the signatures  $I_{11}$  and  $I_{21}$ , respectively, while coefficients  $\xi_1$  and  $\xi_2$  represent the relative weight of the quantization error.

Making use of the triangle inequality, it is simple to delimit the coefficients  $\delta_1$  and  $\delta_2$ ,

$$\begin{aligned}
|\delta_1| &\leq \sum_{i=1}^{\infty} \left( \frac{1}{(iN_L - 1)\pi} \left| S_a\left(\frac{(iN_L - 1)\pi}{N_L}\right) \right| + \frac{1}{(iN_L + 1)\pi} \left| S_a\left(\frac{(iN_L + 1)\pi}{N_L}\right) \right| \right) \\
|\delta_2| &\leq \sum_{i=1}^{\infty} \left( \frac{1}{(iN_L - 1)\pi} \left| S_a\left(\frac{(iN_L - 1)\pi}{N_L}\right) \right| + \frac{1}{(iN_L + 1)\pi} \left| S_a\left(\frac{(iN_L + 1)\pi}{N_L}\right) \right| \right)
\end{aligned} \tag{A4.5}$$

Equation (A4.5) gives a very pessimistic estimation, but even with this estimation, for typical values of  $N_L$  it is easy to show that  $|\delta_{11}|, |\delta_{21}| \ll 1$ , and even more important, for typical values of  $M$ ,  $N$ , and  $A_1$ , it is verified that,

$$\begin{aligned}
|\delta_1| &\ll |\xi_1| \\
|\delta_2| &\ll |\xi_2|
\end{aligned} \tag{A4.6}$$

According to (A4.6) the error in the signatures due to the replicas contribution is masked by the unavoidable error due to the quantization in the analyzer.

To give a sense of the involved numbers, considering the actual test conditions in the proposed setup ( $N=96$ ,  $N_L=16$ ) the error coefficients  $\delta_1$  and  $\delta_2$  due to the spectral replicas are below  $2 \times 10^{-4}$ ,


while the error terms  $\xi_1$  and  $\xi_2$  due to the quantization error are around  $1 \times 10^{-3}$  for  $M=100$ , an order of magnitude above  $\delta_1$  and  $\delta_2$ , and these numbers were obtained for the worst case of feeding directly a discrete-time signal to the analyzer. It can be concluded that, as pointed by (A4.6), the effect of the spectral replicas over the measurements is negligible with respect to the quantization error.


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