Article

Class AB Voltage Follower and Low-Voltage Current Mirror with Very High Figures of Merit Based on the Flipped Voltage Follower

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Abstract: The application of the flipped voltage follower to implement two high-performance circuits is presented: (1) The first is a class AB cascode flipped voltage follower that shows an improved slew rate and an improved bandwidth by very large factors and that has a higher output range than the conventional flipped voltage follower. It has a small signal figure of merit $FOM_{SS} = 46$ MHz pF/μW and a current efficiency figure of merit $FOM_{CE} = 118$. This is achieved by just introducing an additional output current sourcing PMOS transistor (P-channel Metal Oxide Semiconductor Field Effect Transistor) that provides dynamic output current enhancement and increases the quiescent power dissipation by less than 10%. (2) The other is a high-performance low-voltage current mirror with a nominal gain accuracy better than 0.01%, 0.212 Ω input resistance, 112 GΩ output resistance, 1 V supply voltage requirements, 0.15 V input, and 0.2 V output compliance voltages. These characteristics are achieved by utilizing two auxiliary amplifiers and a level shifter that increase the power dissipation just moderately. Post-layout simulations verify the performance of the circuits in a commercial 180 nm CMOS (Complementary Metal Oxide Semiconductor) technology.

Keywords: buffer; flipped voltage follower; CMOS analog integrated circuits; current mirror

1. Introduction

Two of the basic building blocks of analog integrated circuits are the voltage follower and the current mirror. The conventional common-drain amplifier or voltage follower (denoted here as CONV_VF)) [1–3] of Figure 1a has been used for many years as a buffer due to its infinite input resistance, medium–low output impedance $R_{out} = 1/g_m$ (in the order of tens of kΩs) close to the unity voltage gain, and relatively high bandwidth $BW = g_m/(2\pi C_L)$. The flipped voltage follower of Figure 1b [4] is an improved voltage follower that uses local negative feedback to provide lower output resistance $R_{out} = 1/[g_m(g_m r_o)] = 1/(g_m A)$ (hundreds of Ω), where C_L is the load capacitance, g_m and r_o are the transconductance gain and output resistance, and $A = g_m r_o$ is the intrinsic gain of the MOS transistor. The basic Flipped Voltage Follower(FVF) version of Figure 1b (denoted here as CONV_FVF) suffers the serious limitation that it has a very low peak-to-peak output swing $V_{oswingpp}$, which is independent of the supply voltage and given by $V_{oswingpp} = V_{TH} - V_{DSsat}$ (where V_{TH} is the threshold voltage and V_{DSsat} is the drain-source saturation voltage of M_{FVF}). It operates in class A with a peak positive output current and positive slew rate limited by the bias current I_{bias} to a value $SR^+ = I_{bias}/C_L$. Several versions of the flipped voltage follower have been reported with improved output range and lower output resistance. For example, the cascode FVF (denoted here as CONV_CSCFVF) shown in Figure 1c and

reported in [5] uses an additional branch with a cascode transistor M_{CAS} that increases the local feedback loop gain and provides even lower output resistance by a factor $A = g_m r_o$ so that, in this circuit, $R_{out} = 1/[g_m(g_m r_o)^2] = 1/[g_m A^2]$ (on the order of tens of Ωs). It also has an increased output swing, which is dependent on the supply voltage and given by $V_{outswingpp} = V_{DD} - (V_{GS} + V_{DSsat}) = V_{DD} - V_{TH} - 2V_{DSsat}$. The cascode FVF of Figure 1c (denoted here as CONV_CSCFVF) is a class A circuit with a positive slew rate seriously limited by the bias current to a value: $SR^+ = I_{bias}/C_L$. Class AB versions of the FVF have also been reported [6–9] to overcome this limitation to a certain degree.
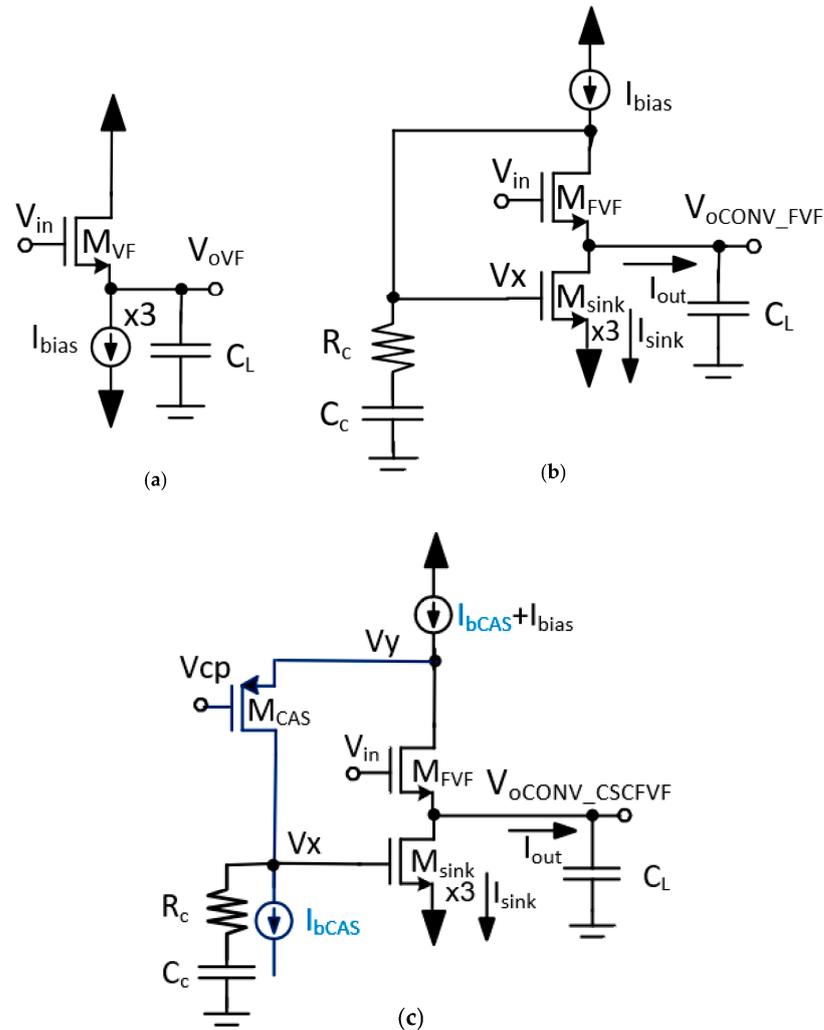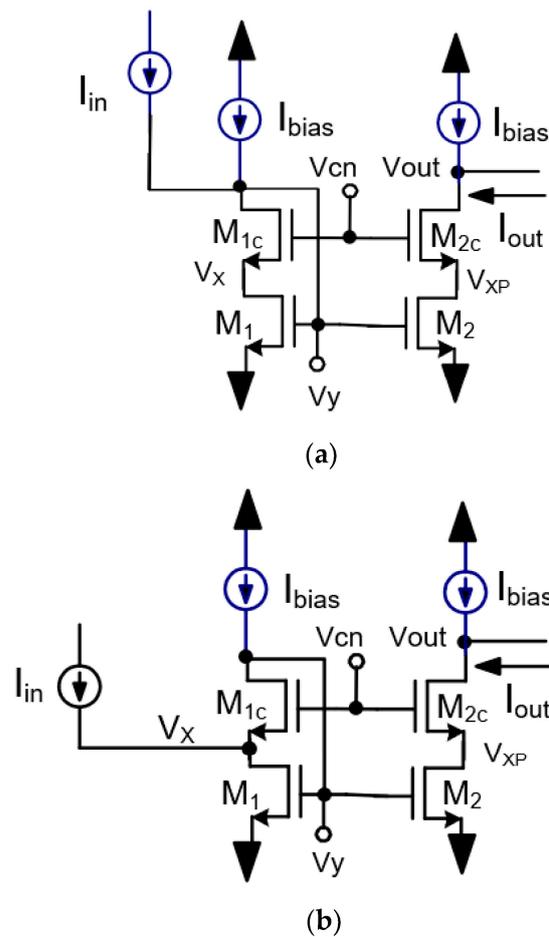

Figure 1. (**a**) Conventional voltage follower, (**b**) basic FVF, and (**c**) cascode FVF.

The low-voltage cascode current mirror of Figure 2a (denoted here as CN_CS_CM) has been used for many years as a high-bandwidth linear current amplifier. It has a moderately low input resistance $R_{in} = 1/g_m$ (on the order of tens of kΩs), moderately high output resistance $R_{out} = r_o(g_m r_o) = r_o A$ (on the order of tens of MΩs), high linearity, low gain error, low output compliance voltage ($V_{outmin} = 2V_{DSSat}$), and moderate input voltage requirements $V_{in} = V_{GS} = V_{TH} + V_{Dssat}$. A simple rearrangement of the circuit of Figure 2a is shown in Figure 2b. It injects the input current source I_{in} at the source of the cascode transistor M_{1C} (node V_x) instead of at its drain (node V_y). This reduces the input voltage requirements from V_{GS} to V_{DSsat} and leads to a reduction in the input resistance by a factor A from $R_{in} = 1/g_m$ to $R_{in} = 1/[g_m(g_m r_o)] = 1/[g_m A]$. Notice that, in this circuit, the input transistors M_1 and M_{1C} form a flipped voltage follower with a constant input voltage V_{cn} at the gate of M_{1C} and the current input signal I_{in} injected at the output terminal of the FVF (node V_x). In spite of the improvement in the mirror characteristics, this modification

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suffers from a non-linear current mirror gain resulting from lambda effect and unequal drain source voltages in the input and output transistors M_1 and M_2 of the current mirror. This is due to the fact that the cascode input and output transistors M_{1C} and M_{2C} have unequal drain currents which cause their gate-source voltages to be different. The gate source voltages of M_{1C} and M_{2C} determine the drain-source voltages of M_1 and M_2 and the linearity of the mirror. This effect can be greatly mitigated in a BiCMOS process by replacing the cascode transistors by bipolar transistors.

(a)

(b)

Figure 2. (**a**) Conventional cascode current mirror and (**b**) FVF-based low-voltage cascode current mirror with reduced input impedance.

In this paper, the authors introduce two improved circuits based on the flipped voltage follower: (1) a power-efficient class AB cascode FVF (denoted here as HP_CSCFVF) with high swing, very low output resistance, and essentially higher small signal and large signal figures of merit than previously reported AB FVF versions and (2) a low-voltage high-performance cascoded current mirror (denoted here as HP_CS_CM) with much lower input resistance and much higher output resistance than the conventional current mirror and highly linear gain. The proposed circuits are described in Section 2. Section 3 shows the post-layout simulation results that verify the high-performance characteristics of the proposed circuits, and Section 4 provides the conclusions.

2. Proposed Circuits

2.1. High-Performance Class AB Voltage Follower HP_CSCFVF

2.1.1. Description

Figure 3 shows the scheme of the proposed class AB high-performance cascode FVF (HP_CSCFVF). It is a modification of the class A cascode FVF reported in [5] and is shown

in Figure 1c. It includes an additional branch with a PMOS transistor M_{source} that provides efficient class AB operation. M_{source} has a small quiescent current $I_{Qsource}$, but it can inject positive output currents I_{out} into the load C_L, which are much larger than $I_{Qsource}$. On the other hand, transistor M_{sink} can sink very large negative load currents (also much larger than the quiescent current of M_{sink} given by $I_{Qsink} = I_{Qsource} + I_{bias}$), as is discussed below. The biasing branch has two diode-connected PMOS transistors M_b and M_{bC}. Based on replica biasing, this branch sets the voltage V_y to a value $V_y = V_{DD} - V_{SGb}$ and the gate voltage of M_{source} to a value $V_g = V_y + V_{bat}$, where $V_{bat} = I_{bat}R_{bat}$. The values of I_{bat} and R_{bat} are selected so that V_{bat} has an approximate value $V_{bat} = V_{SDsat} = 0.1$ V. In this case, the quiescent source-gate voltage of M_{source} is given by $V^Q_{SGsource} = V_{SGb} - I_{bat}R_{bat}$. This leads to a quiescent voltage $V^Q_{SGsource} = V_{SGb} - V_{SDsat} \approx V_{TH}$ close to the threshold voltage of M_{source}. This quiescent source-gate voltage sets a relatively small quiescent current $I_{Qsource}$ in M_{source}, which is independent of the supply voltage. A capacitor C_{bat} forms a high-pass filter with R_{bat} and C_{bat}. This is used to transfer fast transient variations from V_x to the gate V_g of M_{source}.
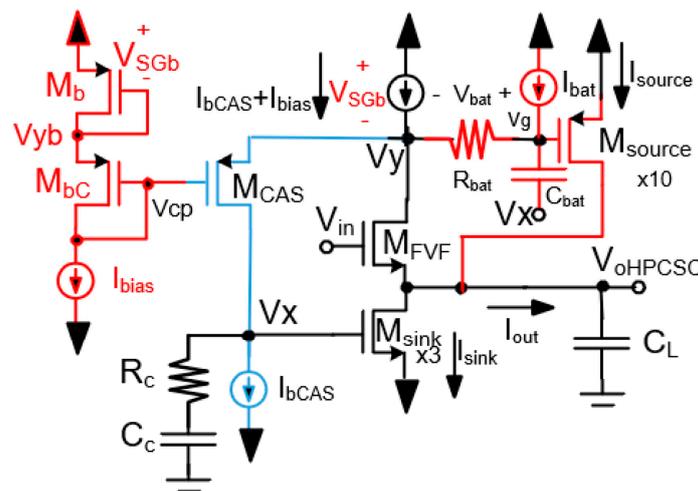

Figure 3. High-performance class AB cascode FVF.

2.1.2. Class AB Operation of Proposed Voltage Follower

For positive input voltage variations in V_{in}, the output voltage V_{oHPCSC} increases, and the gate voltage V_x of M_{sink} decreases. The current in M_{sink} decreases (and eventually turns off) and the dynamic changes in V_x are transferred to V_g by C_{bat} to the gate of M_{source}. The decrease in V_g causes the current I_{source} of M_{source} to increase, providing a positive output current I_{out} that can be significantly larger than the quiescent current $I_{Qsource}$ of M_{source} (in the design described in Section 3, $I_{Qsource}$ has a value $I_{Qsource} = 7$ µA). For negative input voltages, the output voltage decreases, and V_x increases. This increases the current I_{sink} and provides a large negative output current I_{out} that can be much larger than the quiescent current I_{Qsink} of M_{sink}. The FVFs in Figures 1b,c and 3 use an RC compensation network formed by C_c and R_c for the local feedback loop. These elements provide a dominant pole and a high-frequency zero at V_x that approximately match the output pole of the open loop gain $\omega_{pout} = g_{mFVF}/C_L$ at the output node V_{oHPCSC}. This allows FVF circuits to significantly improve their bandwidth with respect to the conventional voltage follower of Figure 1a. This simple but effective FVF compensation and bandwidth extension technique was reported in [10].

2.2. High-Performance Low-Voltage Current Mirror (HP_CS_CM)

The scheme of the proposed low-voltage high-performance current mirror (HP_CS_CM) is shown in Figure 4a. It is a modified version of the FVF current mirror of Figure 2b that includes two auxiliary amplifiers $A_{SEinvfcamp}$ with gain A_{aux} and a level shifter $FVF_{levelshifter}$.

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The transistor level implementation of the auxiliary amplifiers and the level shifter is shown in Figure 4b. Each of the amplifiers form local negative feedback loops with the cascode transistors M_{1C} and M_{2C}. They boost their effective gain by the gain $A_{aux} = (g_m r_o)^2 = A^2$ of the auxiliary amplifiers. They are implemented in Figure 4b using single-ended folded cascode inverting amplifiers formed by M_{FCA1} and M_{CA1} and by M_{FCA2} and M_{CA2}. A modified flipped voltage follower is used to generate a very-low-impedance node V_G that operates as the signal ground (or reference node) for the input common source transistors M_{FCA1} and M_{FCA2} of the auxiliary amplifiers. Transistors M_{BAT}, M_{FCA1}, and M_{FCA2} have the same W/L dimensions, the same quiescent current, and quiescent gate-source voltages. For this reason, the negative feedback loops of the auxiliary amplifiers shown in Figure 4a,b cause the gate voltages V_{refX}, V_X, and V_{XP} to have the same value. This results in equal drain-source voltages of the input and output mirror transistors and leads to a highly linear and accurate current mirror gain. On the other hand, the large gain boosting of the cascode transistors M_{1C} and M_{2C} provided by the folded cascode auxiliary amplifiers leads to an extremely low input resistance $R_{in} = 1/(g_m A^3)/2$, which is lower by a factor of $A_{aux} = A^2/2$ than the input resistance of the FVF mirror of Figure 2b and to an extremely high output resistance $R_{out} = r_o A^3$ that is higher by the same factor A_{aux} than the output resistance of the mirrors of Figure 2. The value of V_{refX} (selected by the designer) sets the input voltage requirement V_{in} of the mirror. It must be higher than V_{DSsat} in order to keep the input and output mirror transistors in saturation. In the proposed design, V_{refX} was selected to have a value $V_{refX} = 0.15$ V, but it can also have been lower since input and output transistors had a value $V_{DSat} = 0.06$ V in the design discussed in Section 3. Remarks: (1) The FVF level shifter is a modified version of the basic FVF (or CONV_FVF). It has a resistor R in series with transistor M_{BFVF}. This resistor R in Figure 4a is used to generate a voltage drop that pulls down the voltage at node V_z and allows transistor M_{BAT} to have enough drain-source ($V_{DS} > V_{DSSat}$) voltage to operate in saturation. (2) The implementation of the auxiliary amplifiers using folded cascode amplifiers with a floating virtual ground node V_G in which the nominal voltage is set by the designer has the purpose of reducing the supply requirements of the circuit. (3) A distinctive characteristic of the proposed mirror is that the modified FVF with resistor R allows the quiescent value of V_G to be set to a value that is convenient to minimize the supply voltage and the input voltage requirements of the circuit. It also allows M_{BAT} to be maintained in saturation. Previous implementations of mirrors with auxiliary amplifiers (i.e., the regulated cascode mirrors discussed in [1]) required the source of the auxiliary amplifier's input transistors to be connected to one of the supply rails and does not allow the supply requirements to be minimized or V_{in} to be set. (4) If required, the gain A_{aux} of the auxiliary amplifiers can be further boosted from a value $A_{aux} = A^2/2$ in the circuit of Figure 4b to a value $A_{aux} = A^3/2$ by utilizing double-cascoded auxiliary amplifiers. This would also boost the output impedance by an additional factor $A/2$ and decrease the input impedance of the mirror by the same factor. (5) The local negative feedback loops formed by the auxiliary amplifiers have only one high-impedance node at V_Y and V_{YP}. Compensation elements R_c and C_c are used to generate a dominant pole (and a zero) at these nodes. This is in order to compensate these loops and to prevent instability. (6) In order to reduce power dissipation, the auxiliary amplifiers and the FVF level shifters are biased with currents I_{bias}/k, which is a factor k times smaller than the bias current I_{bias} of the input and output mirror transistors M_1 and M_2. In the proposed design, a value $k = 10$ was used. This lead to a total quiescent current and power dissipation of the proposed mirror that is only 25% higher than the power dissipation of the mirrors of Figure 2. (7) The proposed current mirror can be easily transformed into a class AB mirror using the techniques reported in [11].

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(**a**)

(**b**)

(**c**)
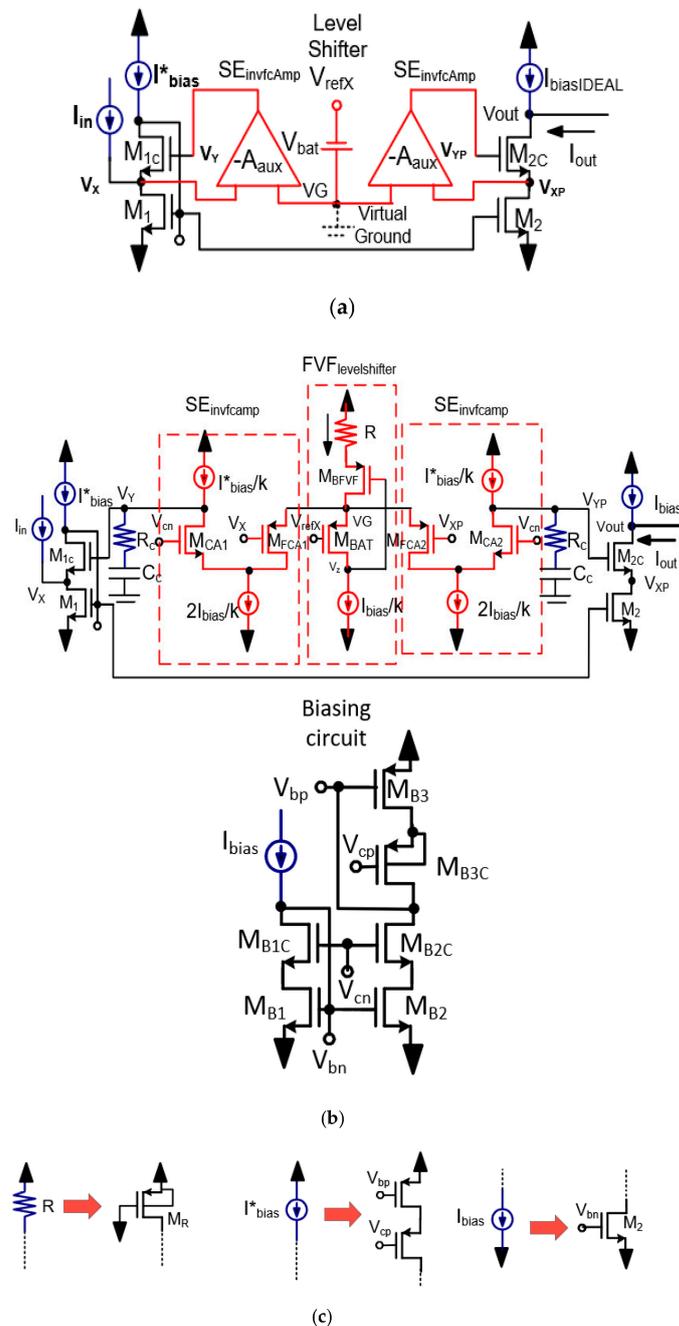
Figure 4. (**a**) Scheme of the proposed low-voltage high-performance current mirror, (**b**) transistor level implementation and biasing circuit, and (**c**) implementation of resistor R, cascode current source I*bias and simple current sources I_{bias}.

3. Simulation Results

3.1. Simulations of the High-Perfromance Class AB Follower HP_CSCFVF

The CONV_VF, CONV_FVF, CONV_CSCFVF, and proposed HP_CSCFVF circuits of Figures 1a–c and 3 were simulated in a commercial 180 nm CMOS technology with dual rail voltages V_{DD} = 0.75 V, V_{SS} = −0.75 V (or V_{supply} = V_{DD} − V_{SS} = 1.5 V), I_{bias} = I_{bCAS} = 5 µA, R_{bat} = 55 kΩ, C_{bat} = 2 pF, I_{bat} = 2 µA, C_L = 100 pF, and W/L = 5/0.2 (µm) for all PMOS, and NMOS transistors, except the PMOS and NMOS transistors, implementing biasing sources that had dimensions W/L = 5/0.4 (µm), values Cc = 0.6 pF, and Rc = 75 kΩ were used. In order to save on silicon area, R_c was implemented with an NMOS transistor with W/L = 0.75/15 and with the gate connected to the positive rail V_{DD}. R_c and C_c were

selected to provide a dominant pole $\omega_{pdom} = 1/R_X C_c$ at node V_X: and a high-frequency zero $\omega_z = 1/R_c C_c$ at V_x that approximately matches at the output pole $\omega_{pout} = g_{mFVF}/C_L$ at the output node V_{oHPCSC} of the FVF, as suggested by the design guidelines in [10]. Transistors M_{source} and M_{sink} were scaled up by factors 10 and 3, respectively. This was performed in order to equalize their dynamic output currents and to achieve symmetrical slew rates (SR+ and SR−). The total quiescent current and power dissipation of the proposed circuit were $I_{TotQ} = 21$ μA and $P_{dissQ} = 31.5$ μW, respectively. The small signal transconductance g_m and output conductance g_{ds} of the NMOS and PMOS unit transistors had the following values: $g_{mN} = 148$ μA/V, $g_{dsN} = 2.94$ μA/V, $g_{mP} = 160$ μA/V, and $g_{dsP} = 2.2$ μA/V.

Figure 5 shows the frequency responses of the CONV_VF, CONV_FVF, CONV_CSCFVF, and proposed HP_CSCFVF. The bandwidth of the HP_CSCFVF is 14.6 MHz, that of the CONV_CSCFVF is 3.47 MHz, that of the CONV_FVF is 2.5 MHz, and that of the CONV_VF is 0.347 MHz. Notice that the bandwidth of the proposed circuit is a factor almost 42 times larger than the bandwidth of the CONV_VF and 4.2 times larger than the CONV_CSCFVF. Figure 6a shows the pulse response of the proposed HP_CSCFVF and of the CONV_CSCFVF to a 1 MHz 0.9 V_{pp} pulse input. Figure 6b shows the corresponding load capacitor currents. It can be seen that the proposed circuit has close to symmetrical positive and negative peak output currents (and consequently slew rate) with the values $I_{outpk}{}^+ = 2.6$ mA and $I_{outpk}{}^- = 2.47$ mA, respectively. Notice that the proposed circuit has peak output currents, which are a factor 118 times larger than the total quiescent current of the circuit. This corresponds to a very large current efficiency factor $CE = I_{outpk}/I_{TotQ} = 118$. The peak currents (and slew rates) of the conventional circuits is much lower due to their class A operation.

The positive and negative slew rates of the proposed circuit are SR+ = 34.47 V/μs and SR− = 34.03 V/μs (for $C_L = 100$ pF). Figure 7 shows the pulse response for various C_L values of 10 pF, 32 pF, 55 pF, 80 pF, and 100 pF. It can be seen that, in all cases, the pulse response has a only a small overshoot. Figure 8 shows the AC response of the output resistance of the proposed circuit. It has a very low value $R_{out} = 2.11$ Ω at low frequencies. The layout of the proposed design is shown in Figure 9. It occupies a 114 μm × 47 μm Si area.
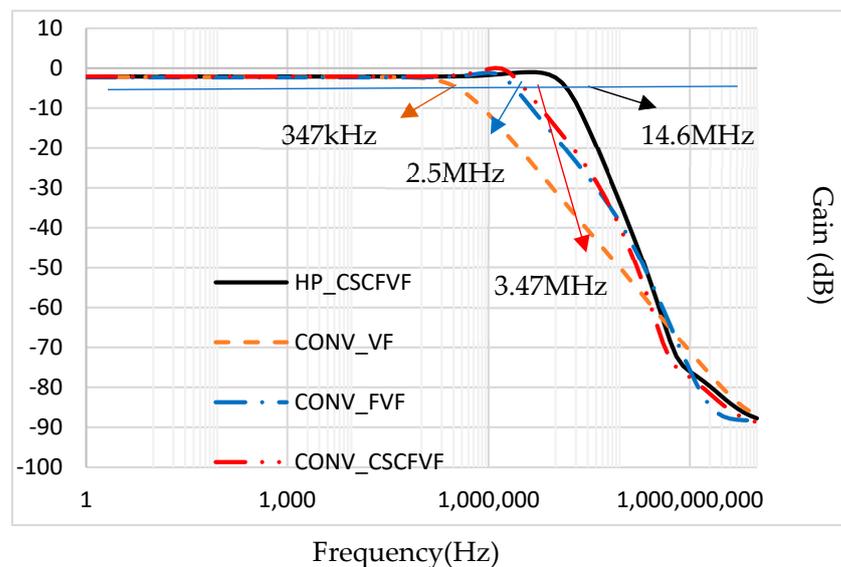

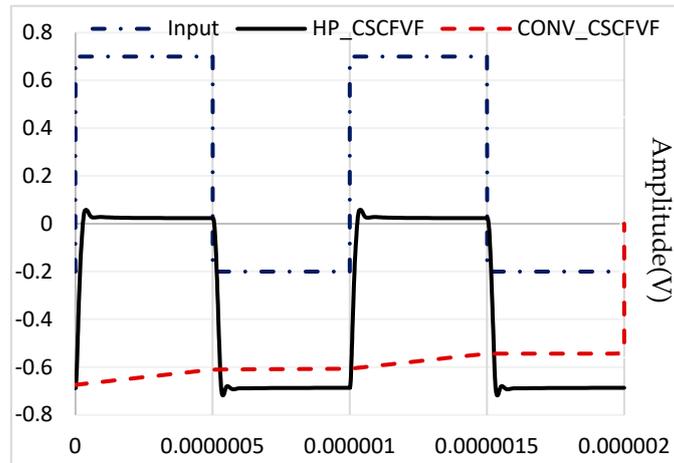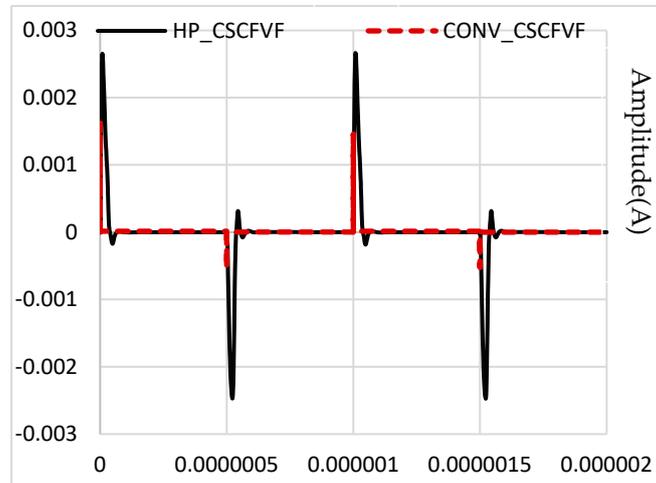**Figure 5.** Frequency Response of the proposed HP_CSCFVF, CONV_VF, CONV_FVF and CONV_CSCFVF.

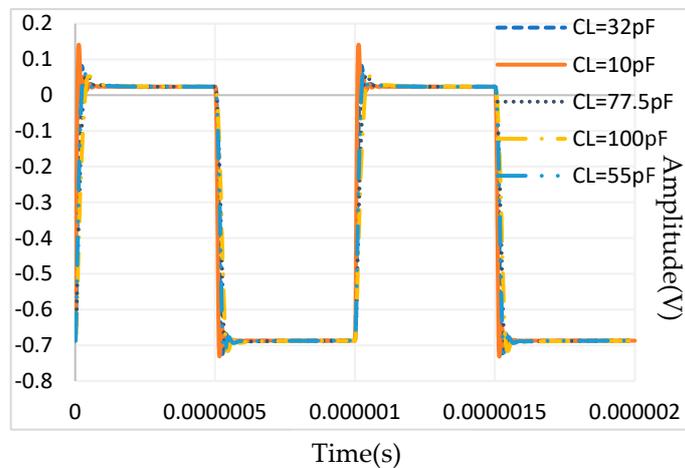**Figure 6.** (**a**) Pulse response of the proposed HP_CSCFVF and CONV_CSCFVF for $C_L = 100$ pF and (**b**) output current of the HP_CSCFVF and CON_CSCFVF at $C_L = 100$ pF.

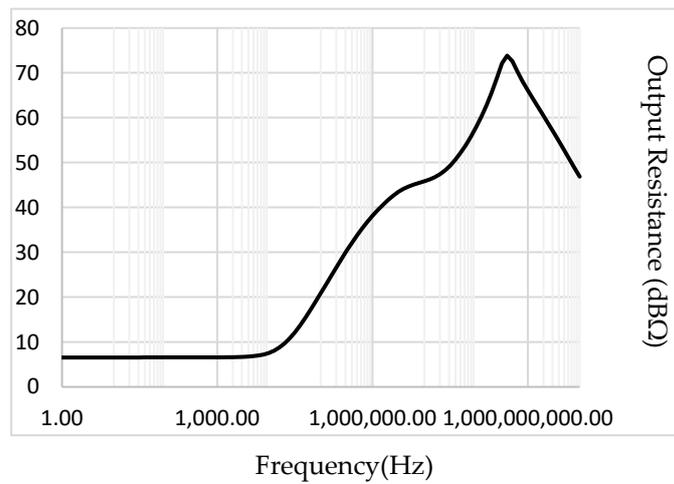**Figure 7.** Pulse response of proposed HP_CSCFVF for load capacitor values: 10 pF, 32 pF, 55 pF, 77.5 pF and 100 pF.

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Figure 8. Output resistance variation with frequency of the proposed HP_CSCFVF.
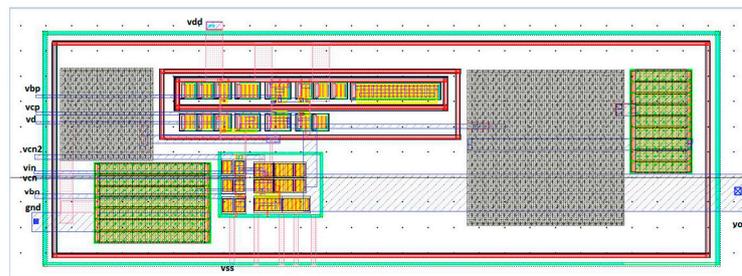

Figure 9. Layout of the proposed HP_CSCFVF.

Table 1A–C show corner analysis of the proposed HP_CSCFVF at three different temperatures (27 °C, 120 °C, and −20 °C). It can be said that the proposed VF's characteristic is very stable against process and temperature variations. The standard deviation (SD) of each parameter for variation in the process has been given in Table 1 for the considered temperatures (27 °C, 120 °C, and −20 °C).

Table 1. (A) Corner analysis at 27 °C; (B) corner analysis at 120 °C; (C) corner analysis at −20 °C.

			(A)			
Corner	tt	ff	fs	sf	ss	SD
I_{TotQ} (µA)	21	22	21	22	21	0.49
f_{3dB} (MHZ)	14.6	18	15.2	14.5	12.5	1.77
SR (V/µs)	24.3	28	21.5	25.6	21.7	2.4
I_{outpk} (mA)	2.68	3.04	2.5	2.7	2.42	0.2
			(B)			
Corner	tt	ff	fs	sf	ss	SD
I_{TotQ} (µA)	26	29	26	27	25	1.35
f_{3dB} (MHZ)	15	18.5	15.2	14.8	12.7	1.86
SR (V/µs)	22.5	25.5	20.18	22.34	20.13	1.9
I_{outpk} (mA)	2.45	2.73	2.38	2.42	2.22	0.16
			(C)			
Corner	tt	ff	fs	sf	ss	SD
I_{TotQ} (µA)	20	20	20	19	19	0.49
f_{3dB} (MHZ)	14.4	17.6	15.8	14.8	12.3	1.74
SR (V/µs)	26.6	29.3	22.9	25.8	22.8	2.4
I_{outpk} (mA)	2.79	3.06	2.67	2.8	2.5	0.18

The THD of the proposed circuit is 0.2% for a 0.5 V_{pp} 100 kHz input signal and 1% for a 0.5 V_{pp} 1 MHz sinusoidal input signal. The equivalent input noise power spectral density and RMS noise are 29 nV/$\sqrt{Hz}$ and 130 μV_{RMS}. The small signal figure of merit is FOM_{SS} = 46 MHz·pF/μW, and the large signal current efficiency figure of merit is $FOM_{CE} = I_{outpk}/I_{TotQ} = MIN\{I_{outpk}+, I_{outpk}-\}/I_{TotQ} = 118$. The global figure of merit is $FOM_{Global} = \sqrt{FOM_{SS}FOM_{CE}} = 73$.

Table 2 shows a comparison of the performance characteristics of the proposed HP_CSCFVF with other voltage followers reported recently in the literature. It can be seen that the proposed HP_CSCFVF has the lowest output impedance, the highest small signal (FOM_{SS}), a large signal and current efficiency (FOM_{CE}), and global (FOM_{Global}) figures of merit in the table.

Table 2. Comparison of the proposed HP_CSCVF with state-of-the-art work.

Parameter	Ref./Year [6]/2012		Ref./Year [12]/2016	Ref./Year [13]/2018	Ref./Year [14]/2016	Ref./Year [15]/2021	Ref./Year [16]/2018	CONV_VF Figure 1a	This Work Figure 3
Process technology (μm)	0.35	0.18	0.18	0.5	0.045	0.5	0.18	0.18	0.18
	Exp	Sim by Auth.	Sim	Exp	Sim	Exp	Sim	Sim	Sim
Supply (V)	3	$\pm$0.9	1.2	1.5	1.2	2	1.2	$\pm$0.75	$\pm$0.75
I_{TotQ} (μA)	81	243	20.8	80	8.3	69	20	9	21
Load Cap. (pF)	20	50	10/100	50	1	47	1	100	100
BW (MHz)	5.8	3.65	15@100 pF	10	170	32	670.2	0.347	14.6
$I_{outpk}+$ (mA)	1.62	3.16	0.32	1.8	0.17	1.59	0.116	0.085	2.6
$I_{outpk}-$ (mA)	1.67	3.16	NA	1.8	0.08	1.42	0.120	0.034	2.47
SR$^+$ (V/μS)	79.4	63.2	32@10 pF	36	42	33.8	116.6	2.5	34.47
SR$^-$ (V/μS)	83.6	63.2	NA	36	50	30.3	120.5	12	34.03
Output resistance (Ω)	NA	NA	56	NA	1.15k	NA	144	1.2k	2.11
Quiescent power P_{dissQ} (μWatt)	243	437	25	120	10	138	24	13.5	31.5
$FOM_{CE} = I_{outpk}/I_{TotQ}$	20	12	15	22.5	10	20	5.8	3.7	118
$FOM_{SS} = BWxC_L/P_{dissQ}$ [(MHz)pF]/μW	0.47	0.42	60	4.16	17	10.9	28	2.5	46
FOM_{Global}	3.06	2.24	30	9.7	13	15	12.7	3.04	73

Figure 10 shows the Monte Carlo (MC) analysis of the proposed HP_CSCFVF power dissipation over 200 sample Monte Carlo simulation for process variation and mismatch. The mean quiescent power is 35.38 μW, and the standard deviation is 0.605 μW. From the corner analysis and Monte Carlo analysis, it can be ascertained that the proposed VF is robust against process variation, temperature, and mismatch effect.

3.2. Simulation Results for Low-Voltage High-Performance Current Mirror HP_CS_CM

The CN_CS_CM and proposed HP_CS_CM current-mirror circuits of Figures 2a and 4 were simulated in a commercial 180 nm CMOS technology with a supply voltage of 1V and I_{bias} = 2 μA. The resistor used to implement R_{bat} in the FVF level shifter has a value 75 kΩ. It is implemented using a PMOS transistor. The W/L ratio of the PMOS and NMOS transistors used in the input and output stages of both current mirrors are W/L = 5 μm/0.4 μm. Transistors used in the auxiliary amplifiers and the FVF level shifter of the proposed current mirror are scaled down by factor k = 10. This was performed in order to reduce the quiescent power dissipation. The compensation elements had values C_c = 1.5 pF and R_c = 4 kΩ.

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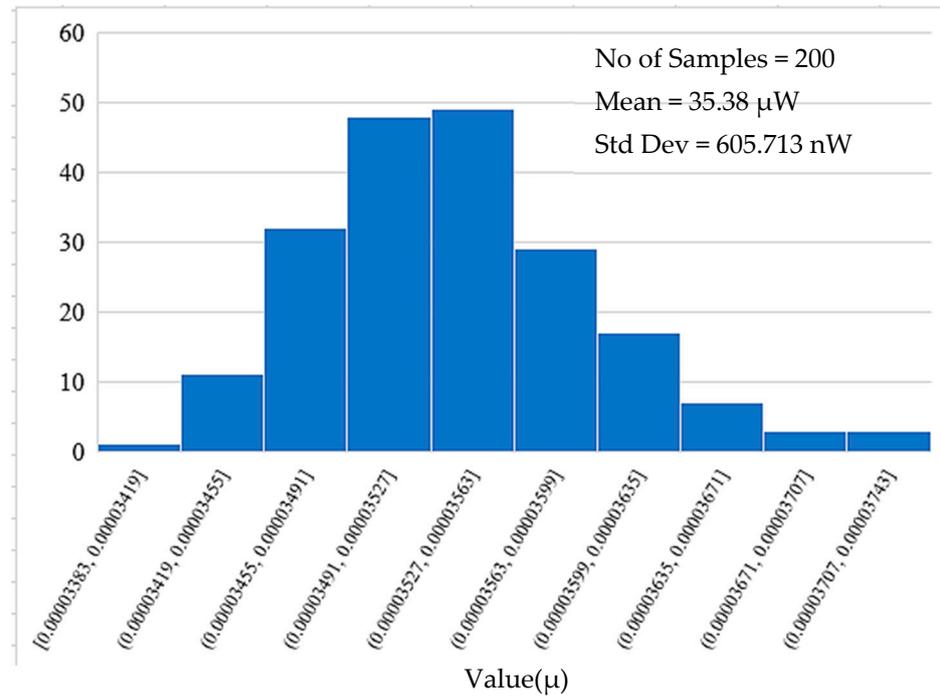
Figure 10. Monte Carlo analysis of the Proposed HP_CSCFVF quiescent power dissipation over 200 samples MC simulation for process and mismatch variation.

Figure 11 shows the frequency response of the proposed high-performance cascoded current mirror (HP_CS_CM). It has a 144 MHz bandwidth. Figure 12 shows the frequency response of the input impedance of the conventional cascode mirror CN_CS_CM and of the proposed HP_CS_CM. The CN_CS_CM has constant input impedance of 22 kΩ, whereas the input impedance of the proposed current mirror is 0.212 Ω up to 800 Hz and 8.9 kΩ at 118 MHz. The HP_CS_CM has an input impedance, at low frequencies, that is close to 10^5 times lower than the CN_CS_CM.
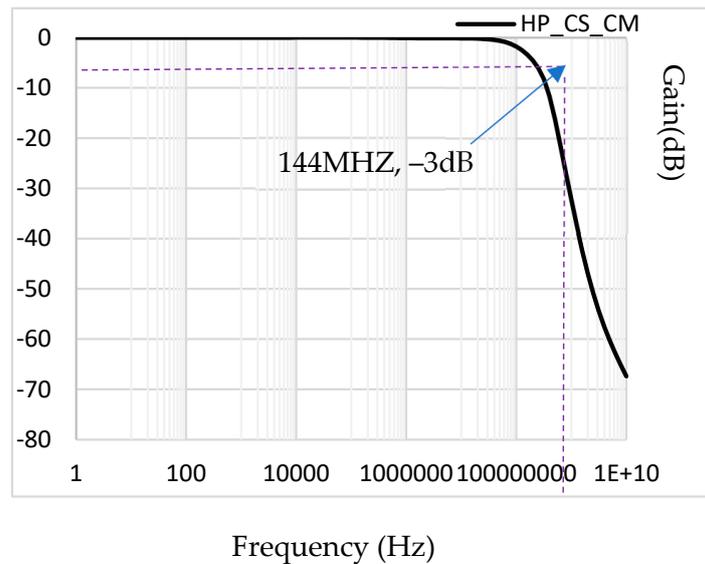

Figure 11. Frequency response of the High performance cascode current Mirror.

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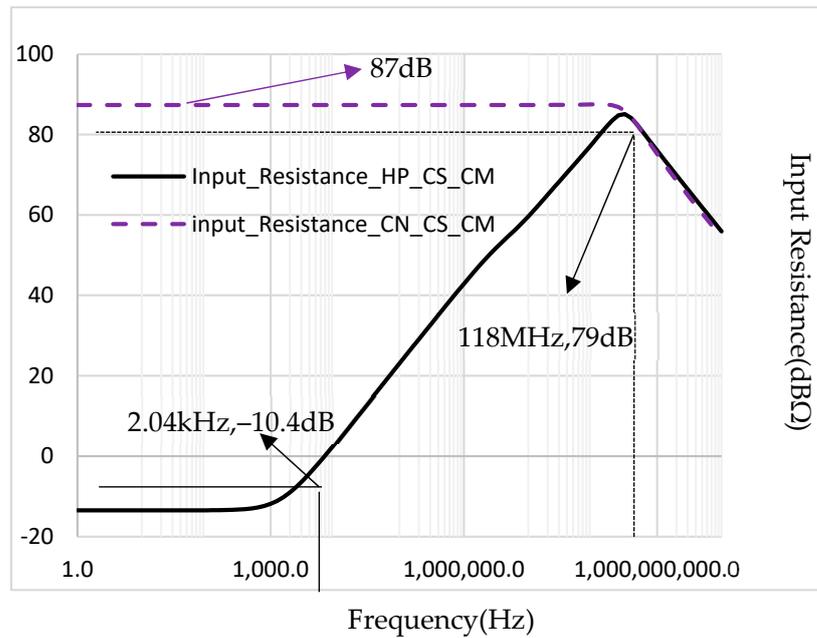
Figure 12. Variation of input resistance with the frequency of Proposed HP_CS_CM and CN_CS_CM.

Figure 13 shows the frequency response of the output impedance of the CN_CS_CM and of the HP_CS_CM. The proposed HP_CS_CM has an output impedance of 112 GΩ until 100 Hz, and the lowest output impedance is 18 MΩ through its bandwidth. On the contrary, the output impedance for the CN_CS_CM is 355 MΩ. Thus, the proposed high-performance current mirror has an output impedance that is 315 times higher than the CN_CS_CM at low frequencies.
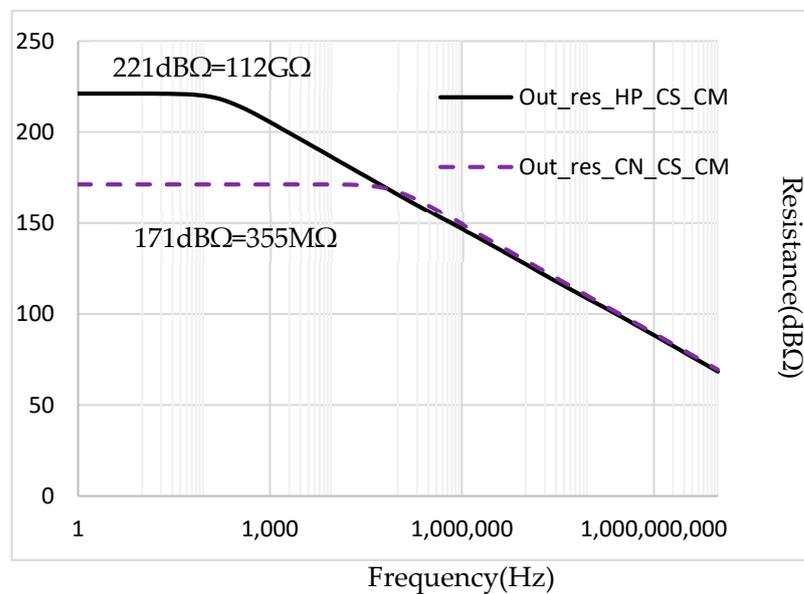
Figure 13. Variation of output resistance with frequency of High Performance HP_CS_CM and CN_CS_CM.

Figure 14 shows the transient response to a triangular input current waveform. It can be seen that the proposed HP_CS_CM closely follows the linear input triangular current waveform. Figure 15 shows the transient pulse response of the proposed HP_CS_CM to a 10 MHz, 10 μA input pulse. It can be seen that the proposed HP_CS_CM has no peaking in the output pulse response.
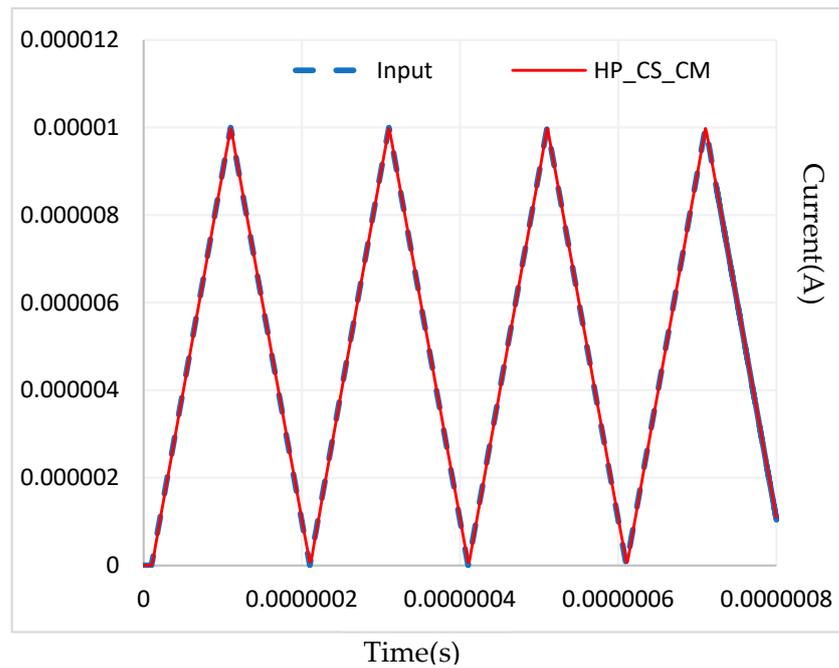
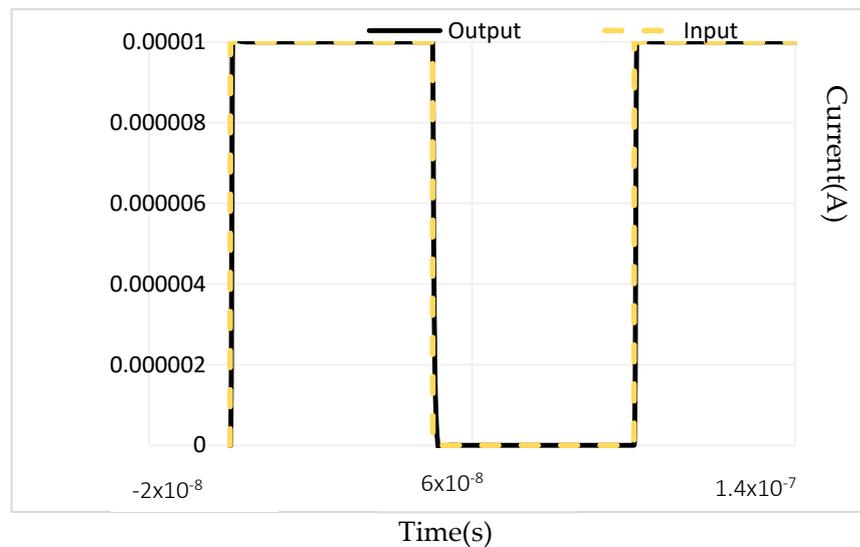**Figure 14.** Transient response of the High performance Current Mirror.

Figure 15. Transient Pulse Response of High-Performance Current Mirror.

An ideal current source is a circuit element that maintains a constant current flow independent of the voltage developed across its terminals as this voltage is determined by other circuit elements. To verify this property, Figure 16 shows the DC output transfer characteristics for dc voltage variation of 0 to 1 V by stepping the input current up from 0 to 10 μA in steps of 2.5 μA. It can be seen that the mirror compliance (minimum output) voltage for performance as a current source is approximately 0.2 V.

Figure 17 shows the input voltage of the CN_CS_CM and of the proposed HP_CS_CM by sweeping the input current I_{in} from o to 10 μA. It can be seen that the proposed HP_CS_CM has a constant 0.15 V input voltage, while the input voltage of the conventional mirror CN_CS_CM varies from 450 mV to 550 mV.
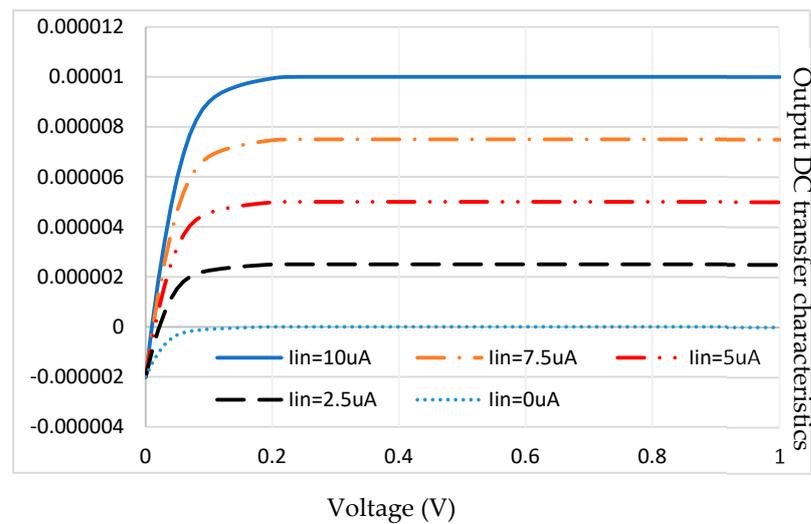
Figure 16. Output DC transfer characteristics of HP_CS_CM V_{outmin} = 0.2 V.
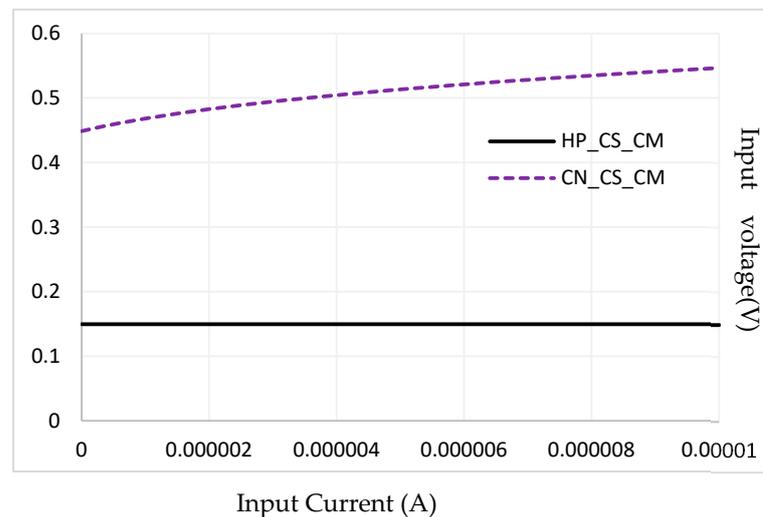

Figure 17. Input voltage with variation of input current.

Figure 18 shows the gain error (in percent) e = $100[(I_{out} - I_{in})/I_{in}]$ in the current transfer characteristic of the CN_CS_CM and the proposed HP_CS_CM as a function of the input current. It can be seen that, as expected, errors are similar since, in both mirrors, the drain-source voltages of input and output transistors are very similar. The total harmonic distortion of the proposed HP_CS_CM is given in Table 3 for a 200 μA amplitude sine wave at frequencies 500 Hz, 10 KHz, 1 MHz, and 100 MHz.

Table 3. Variation in THD with frequency for HP_CS_CM at different frequencies with 200 μA amplitude sinusoidal current.

Frequency (Hz)	THD (dB)
500	−60
10 k	−62
1 M	−60
100 M	−40

A Monte Carlo analysis with 200 samples was executed for some important parameters of the proposed HP_CS_CM for a 2 μA bias current. Table 4 gives the mean value and standard deviation of the bandwidth, input, output resistance, quiescent power, and gain

for 200 runs. It can be see that the proposed current mirror is robust against process variation and mismatch effects. A noise analysis was also performed for the HP_CS_CM. The input referred noise was 14.5 pA/$\sqrt{\text{Hz}}$.
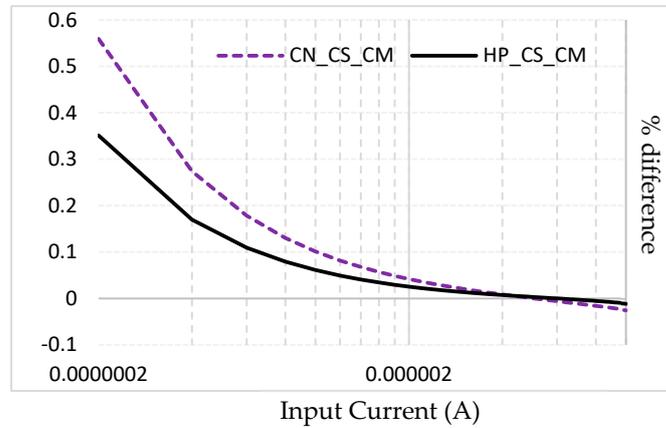

Figure 18. Error in current transfer characteristic of the CN_CS_CM and HP_CS_CM.

Table 4. Summary of results of 200 samples Monte Carlo analysis of proposed current mirror's parameter.

Parameter Name	Mean Value	Standard Deviation
Bandwidth (MHz)	144	0.789
Input resistance (dBΩ)	−13.7	0.728
Output Resistance(dBΩ)	221	0.505
Quiescent Power (μW)	5.33	0.066
Gain (A/A)	0.999	17.8 μ

Table 5 compares the performance characteristics of the proposed HP_CS_CM to other low-voltage mirrors in the literature [17–20]. The proposed mirror has the highest output resistance and the lowest input resistance of all mirrors. Bandwidth is dependent on power dissipation. A mirror figure of merit FOM$_{CM}$ = BW/P$_{diss}$ is used to compare the circuits. Notice that the proposed mirror has the highest FOM$_{CM}$ in the table (the input compliance voltage of the resistance based mirror in [18] is lower but it has the serious shortcoming that, with the reported 39.6 mV input voltage, it is subject in practice to very large random gain/linearity errors caused by mismatch in V$_{DS}$ due to random offset of input and output transistors in the control circuit).

Table 5. Comparison of the proposed HP_CS_CM with state-of-the-art work.

Parameter	[17]	[18]	[19]	[20]	This Work
Input Compliance Voltage	520 m	39.6 m	-	-	150 m
Current Transfer error (%)	1.71	0.6	0.16	0.22	0.1
Input resistance (Ω)	21.43	496	68.3	130	0.212
Output Resistance (Ω)	1.14 G	1 M	10.5 G	9.5 G	112 G
Bandwidth (Hz)	6.17 G	181 M	402 M	2.7 G	144 M
Noise (pA/$\sqrt{\text{Hz}}$)	-	-	7.8	-	-
Supply (V)	1	0.9	1	1	1
Power (μW)	916.65	154	110	142.9	5
FOM$_{CM}$ (MHZ/μW)	6.73	1.17	3.6	18.89	28.8
Technology (μm)	0.18	0.18	0.18	0.18	0.18

4. Conclusions

Two high-performance circuits based on the flipped voltage follower were introduced: (1) One was a class AB high-performance cascode flipped voltage follower that uses an additional output branch with a PMOS current-sourcing transistor. Replica biasing techniques are used to bias the sourcing transistor with a small quiescent current independent of the supply voltage. Under dynamic conditions, the sourcing transistor can provide very large positive output currents, which are over a factor 100 larger than the total quiescent current of the proposed circuit. Simulations in a commercial 0.18 μm CMOS technology have shown that it has low supply voltage requirements, greatly enhanced bandwidth, approximately symmetrical and large slew rates, and the largest small signal and large signal figures of merit of all class AB voltage followers. (2) The other was a low-voltage high-performance current mirror with 0.15 V input and 0.2 V output compliance voltages, 1 V supply voltage, extremely high output resistance (112 GΩ), extremely low input resistance (0.212 Ω), and the highest figure of merit.

This high-performance current mirror is implemented by utilizing two auxiliary amplifiers and a level shifter that boost the gain of the mirror cascode transistors and that equalize the drain source voltages of input and output mirror transistors. The auxiliary circuit increases the power dissipation of the mirror by only 25%. These characteristics were also verified with simulations in a commercial 0.18 μm CMOS technology.

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